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A TURN-OFF

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START WITH THE RIGHT OP AMP WHEN DRIVING SAR ADCs

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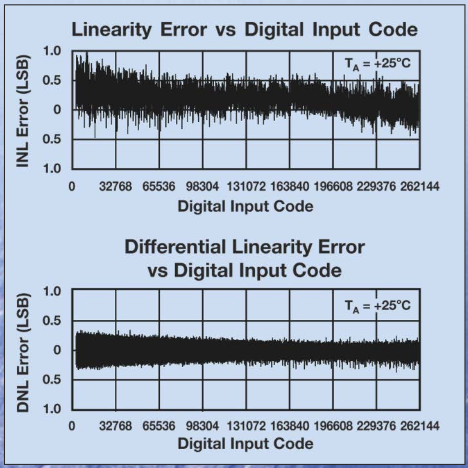

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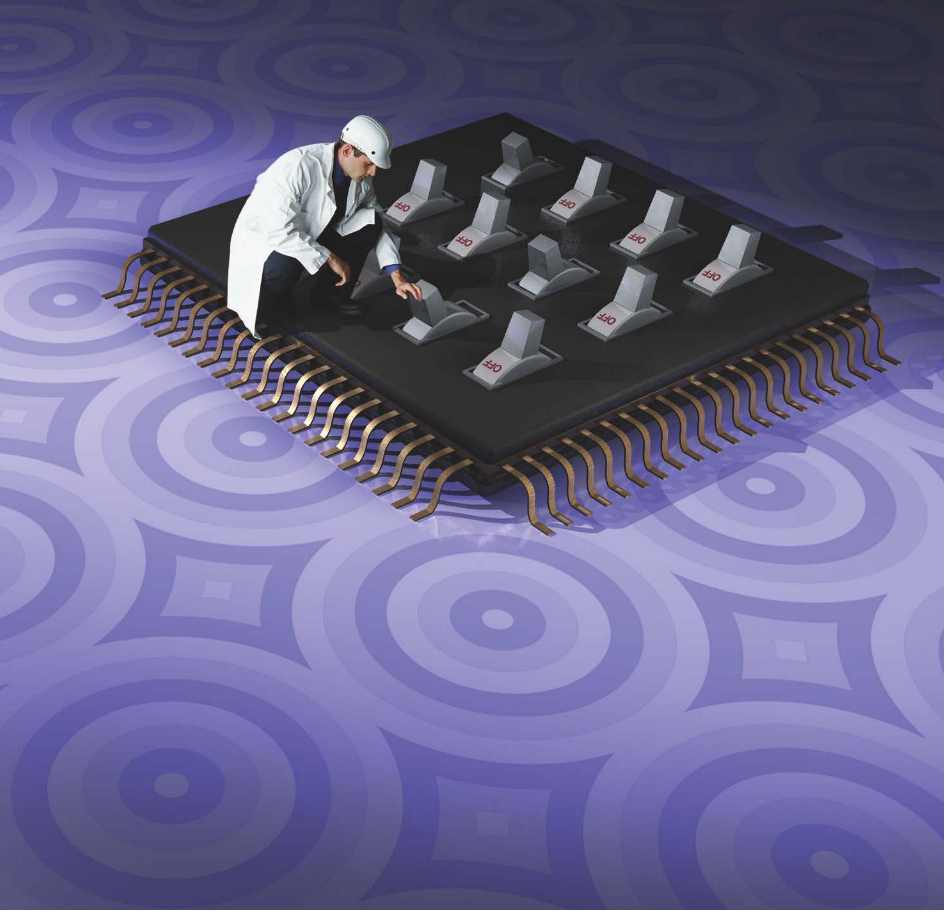

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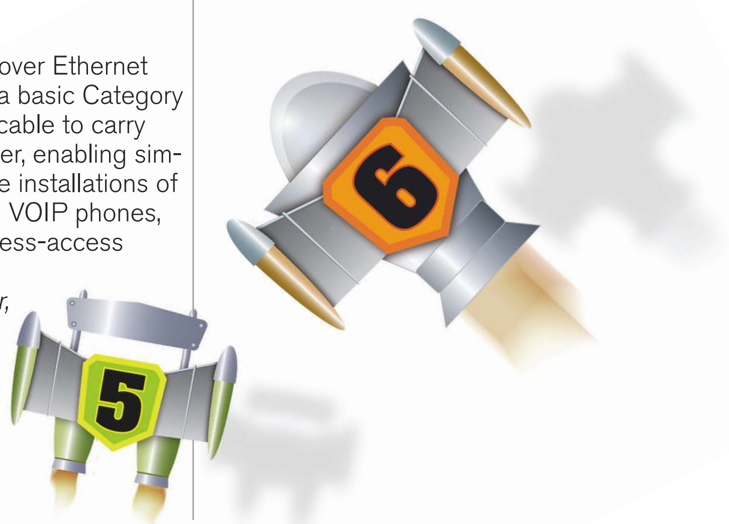

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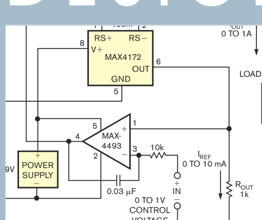

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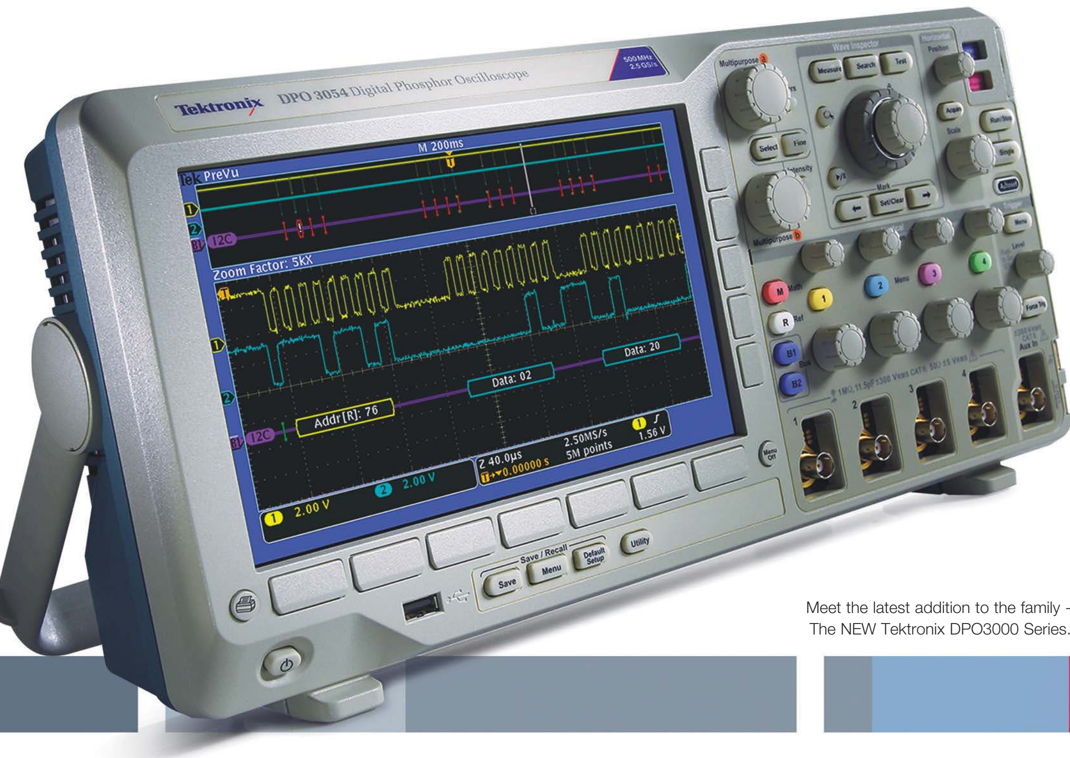

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Record Length	10 M points on all channels
Sample Rate	Up to 5 GS/s on all channels
Display	10.4 in. (264 mm) XGA
Serial Bus Trigger and Decode	I²C, SPI, RS-232/422/485/UART, CAN, LIN, FlexRay

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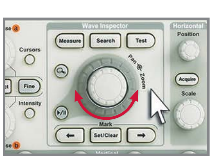
Serial Bus Trigger and Decode	I²C, SPI, RS-232/422/485/UART, CAN, LIN



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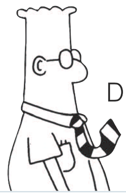

DEPARTMENTS & COLUMNS

PRODUCT ROUNDUP

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ARM develops IP for Common Platform alliance 32-nm, 28-nm nodes
ARM will develop and license a platform of physical IP (intellectual property) for the IBM-led Common Platform alliance as the group moves its SOC work to the 32- and 28-nm nodes based on high-k metal-gate technology.
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Toshiba, SanDisk look to expand digital-media delivery via SD cards
The two memory rivals separately announced partnerships that encourage the use of SD cards for the download and purchase of digital media.
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Android phone announced; platform expected to gain 4% of US fourth-quarter smartphone share
The Google branding behind T-Mobile's G1 Android-based smartphone will take it and the platform only so far, analysts say.
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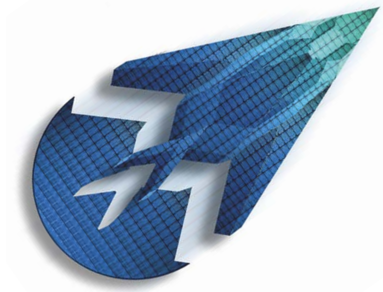

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A selection of recent articles receiving high traffic on www.edn.com.

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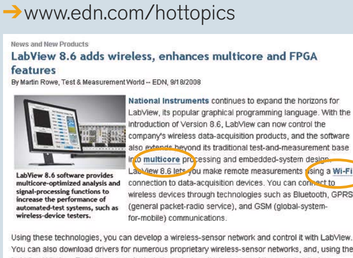
News and New Products

LabView 8.6 adds wireless, enhances multicore and FPGA features

By Martin Rowe, Test & Measurement World -- EDN, 9/18/2008

LabView 8.6 software provides multicore-optimized analysis and signal-processing functions to increase the performance of automated-test systems, such as wireless-device testers.

National Instruments continues to expand the horizons for LabView, its popular graphical programming language. With the introduction of Version 8.6, LabView can now control the company's wireless data-acquisition products, and the software also extends beyond its traditional test-and-measurement base into multicore processing and embedded-system design. LabView 8.6 lets you make remote measurements using a Wi-Fi connection to data-acquisition devices. You can connect to wireless devices through technologies such as Bluetooth, GPRS (general packet-radio service), and GSM (global-system-for-mobile) communications.

Using these technologies, you can develop a wireless-sensor network and control it with LabView. You can also download drivers for numerous proprietary wireless-sensor networks, and, using the LabView Wireless Toolkit, you can test wireless devices that use any of these technologies.

BY PAUL RAKO, TECHNICAL EDITOR

White spaces and black hearts

Google co-founder Larry Page is still pushing radio white-space proposals (**Reference 1**). *White space* refers to the unused television channels in a region, along with the spectrum-guardband buffer between channels. Page makes the absurd claim that small devices, such as his new G1 phone, cannot possibly cause white-space interference. He calls recent tests on white space "rigged" and "despicable" because the testers conducted research on wireless-microphone-interference avoidance while using nearby TV frequencies.

I remember the days when Google's mantra was "Do no evil." I suspect that Page, referring to Google's "Free the Airwaves" publicity campaign, thinks he is doing no evil—perhaps even doing good—by helping the people. I agree that the telecommunications industry has a history of despicable behavior. And, although the industry needs to address the high costs of cell-phone plans and the associated poor quality and lousy service, Page is wrong to call broadcasters despicable for fighting something that almost certainly causes TV interference.

Some analog engineer should explain to Page that the size of a device has nothing to do with interference. A few watts from a cell phone are enough to interfere with the microvolt TV signals your tuner is trying to pick up. The real problem lies with the base stations. Unless the White Spaces Coalition Wireless Innovation Alliance (www.wirelessinnovationalliance.org) proposes to make a device-to-device mesh network, it will need base stations, just as any other cell-radio system needs base stations. And, unless the coalition proposes to put those base stations into satellites, the base stations will be near a bunch of TV receivers. A lot of neat charts show that radio transmissions occupy only a small slice of guardband, but RF artifacts, including side-lobe and multipath effects—inherent in the real-world transmission of radio waves—will occur with white-space broadcasts, too.

It is madness to propose the introduction of any potentially interfering devices until after the rollout of digital TV next February. My experience is that digital is not all that it is cracked up to be. A plane landing nearby or someone using 802.11 or unlicensed devices seems to cause problems with some digital TV broadcasts. Other digital broadcasters' signals are so weak that the broadcasts keep dropping out and become unwatchable. Analog transmissions from the same broadcaster may come in "snowy," but the audio is crystal-clear and you can still watch the broadcast. Like most other things of a digital nature, it is perfect when it works, but let's wait until we see how delicate these digital-TV transmissions are before we put even more interfering devices into the same frequency bands.

Page may want to consider the social-class component of all these proposals. Millions of people in the United States cannot afford cable or satellite TV. They won't be buying a smartphone, and they won't be using Google to find coffee shops selling lattes with just the right amount of foam. These people are living from paycheck to paycheck, and the one respite they get after a day's work may be watching free broadcast television. Just because Google and the cell-phone companies have better lobbyists and more money than the broadcasting industry is no reason to abuse these people.

The Federal Communications Commission (www.fcc.gov) has become less concerned about interference and more concerned about money. It has gone from being a technical organization to being a political one. With modern-day fiscal disasters, such as the war in Iraq and the collapse of the housing market, the FCC is under even more pressure to add to the revenue stream. Nevertheless, the industry should put white-space transmissions on hold until we see how badly the digital-TV rollout hurts broadcast television. The cell-phone companies engineered one rip-off of US citizens with digital TV. Let's not allow the Web-search and computer companies to pull off another one. **EDN**

REFERENCE

1 Whoriskey, Peter, "Update: Google Guy's Words Get Quick Response," *The Washington Post*, Sept 24, 2008, http://voices.washingtonpost.com/posttech/2008/09/google_guy_white_spaces_test_r.html?hpid=sectech.

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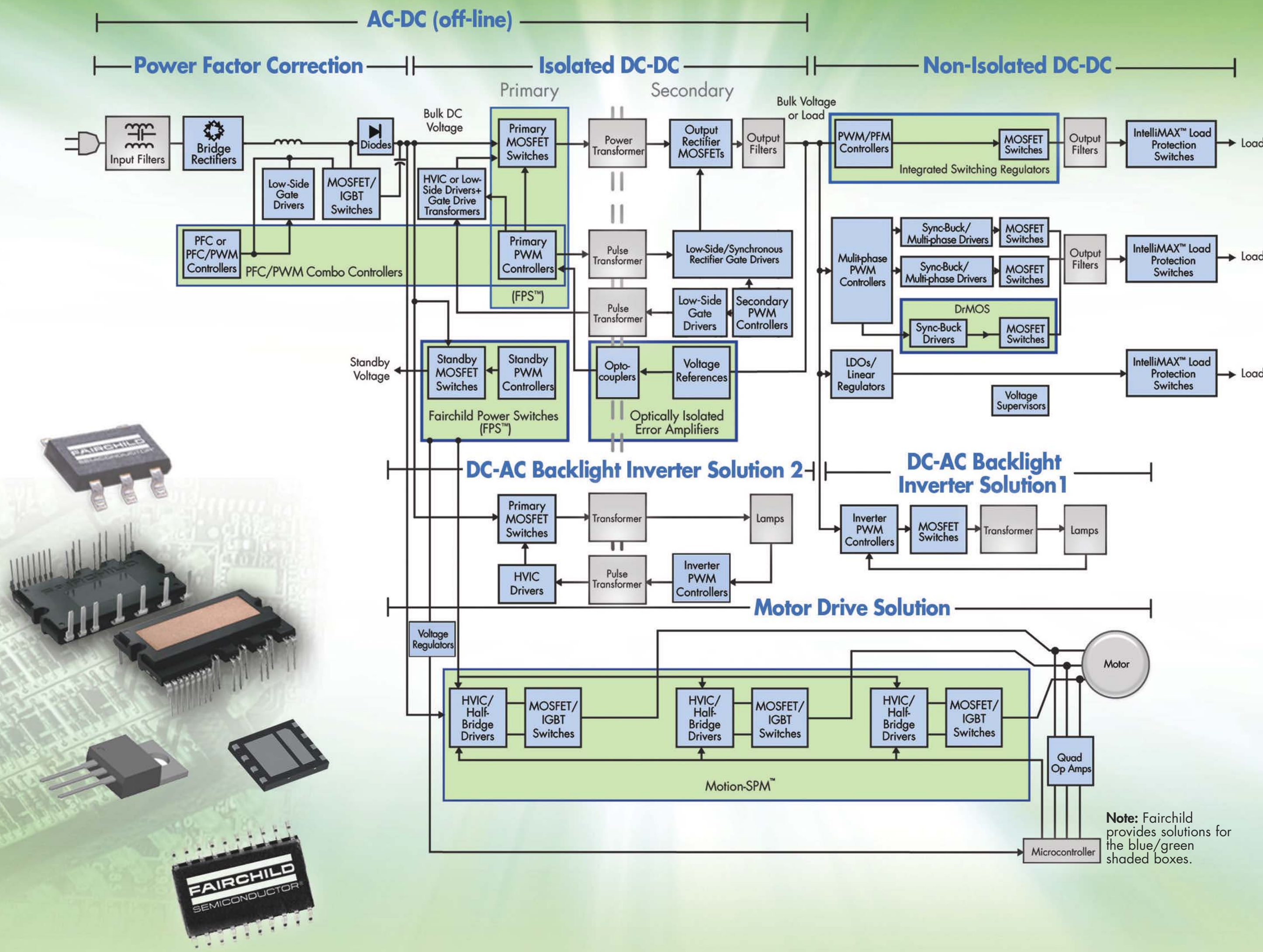

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AC/DC-power supply ups power density with innovative magnetics, digitally controlled modules

Incorporating a new dual-function-transformer design, digitally controlled modules, and an online product configurator, a new series of digitally controlled power modules joins Lambda's NV-Power (www.nv-power.com) line. The modules feature a magnet device comprising two transformers on one core. The device alternates as a transformer and an inductor and is integral to the supply's synchronous-rectification process. Lambda claims that the transformer is 20% smaller and delivers 30% more power than conventional designs.

The digitally controlled modules allow customization based on an application's requirements, such as modified current-limit or start-up characteristics. Using the NV-Power configurator, designers can create their own configuration online, and the tool checks the configuration and suggests the optimal approach. The series uses an 8-bit Atmel (www.atmel.com) microcontroller to handle housekeeping routines and replace many of the comparators, op amps, and other otherwise-necessary discrete components, resulting in a 50% parts-count reduction. Power density for the series is as high as 19W/in.^{3}. All units operate with an input range of 90 to 264V ac.

The Lambda NV-Power series features a new dual-function-transformer design that alternates transformer and inductor functions. The NV-700 series provides as much as 700W of output power; the NV-350 series provides as much as 350W of output power.

The NV-350 series provides as much as 350W of output power with less-than-180V-ac mains and as much as 660W continuous, or 740W peak for 10 seconds, with greater-than-180V-ac mains. As many as six user-selectable outputs fit into a 1.6×3.75×10.8-in. package. The NV-700 series provides as much as 700W of output power with less-than-150V-ac mains and as much as 1150W continuous, or 1450W peak for 10 seconds, with greater-than-150V-ac mains. As many as eight user-selectable outputs fit into a 1.6×4.92×10.8-in. package.

The series targets the instrumentation, medical-equipment, server, and security-network markets and is available now with prices starting at $214 each (100), depending upon the configuration.

—by Margery Conner

▷**Lambda Power**, www.lambdapower.com.

$1799 mixed-signal scope takes 1G sample/sec/channel in real time

Link Instruments' $1799, PC-based MSO (mixed-signal oscilloscope)-9212 features 1G-sample/sec real-time sampling, or 50G samples/sec for repetitive signals, and a 2 million-point/channel data buffer with fully synchronized and cross-triggered analog- and digital-waveform acquisition.

The unit provides 14 channels—two for analog inputs and 12 for logic inputs. The input samplers' bandwidth is 200 MHz for the analog-input channels and 150 MHz for the logic-analysis channels. Advanced triggering options include rising/falling edge, 12-bit logic, I^{2}C (inter-integrated circuit) and SPI (serial-peripheral-interface) buses; pulse width and count; and pulse-window mode, which triggers on pulses within specified parameter ranges.

The $1799, PC-based MSO-9212 mixed-signal oscilloscope comprises the main unit (left), on which you find the two analog inputs and the trigger input; the logic pod (right), which acquires signals from the 12 logic inputs; and a tiny ac/dc-power supply (not shown).

The lightweight, 7.9×4.7×1.5-in. MSO-9212 connects to a PC through a high-speed USB 2.0 port. The 12-channel digital-input module, or logic pod, measures 4.25×3.87×0.8 in., and the ac/dc-power supply measures 2.1×1.8×1.1 in., not including the ac-power-input blades that project from it and plug into the ac source. For more details, go to www.edn.com/article/CA6596985.**—by Dan Strassberg**

▷**Link Instruments Inc**, www.linkinstruments.com.

Low-cost, 60- to 300-MHz DSOs offer deeper memory, more features

Buyers at the low-priced end of the DSO (digital-storage-oscilloscope) market may not demand breakthrough features or bandwidths beyond 10 GHz, but they do insist on solid value, ruggedness, and ease of use. Those who have only approximately $1000 to $2300 to spend on a scope can't allow themselves the temptations of such niceties as extended DSP capabilities or bandwidths and screen sizes greater than their requirements—unless they can get those attributes at prices within their budgets. For the last two and a half years, the lowest-priced series in LeCroy's broad line of scopes has been a family of two- and four-channel instruments with bandwidths of 100 to 500 MHz and US prices that begin at approximately $3000. Unhappily for the company, those scopes' elegant features didn't attract many of the shoppers who had been searching for instruments at half that price, especially when several well-known competitors offered more basic products at the desired prices.

All members of the WaveAce family include 5.7-in.-diagonal color LCDs, a front-panel USB-host port for memory sticks, and a rear-panel USB-device port for connecting to a PC. The distinctive dark front panel makes the units easily recognizable.

LeCroy's announcement of the WaveAce family of 60- to 300-MHz, two-channel real-time scopes changes the situation and provides buyers with enhanced performance and features without exacting a price penalty. The family includes a 300-MHz unit, whereas the competitive low-cost families top out at 200 MHz. WaveAce scopes make automated measurements of 32 waveform parameters, whereas competitive units make such measurements on only 11 parameters. In the 200- and 300-MHz units' 2G-sample/sec, single-channel, interleaved-sampling mode, WaveAce units capture records as deep as 16k samples, whereas competitive units offer only 2.5k or 4k samples. (At the time of LeCroy's press briefing, it was unclear whether the first units the company shipped would include the 16k-sample memory depth or whether the maximum memory depth would initially be 8k samples. In that scenario , purchasers of the initial units will be able to upgrade at no cost and without hardware modifications when the 16k-sample feature becomes available; downloading the firmware upgrade will take about five minutes, and installation will take five more minutes.) Moreover, all WaveAce units offer color displays, whereas one competitor offers a mix of color and monochrome. The 5-lb WaveAce units occupy a space that is only 5 in. deep on your benchtop; the units of one competitive family are more than twice as deep.

The WaveAce family includes six members, two with 60-MHz bandwidth, two with 100-MHz bandwidth, one with 200-MHz bandwidth, and one with 300-MHz bandwidth. One 60-MHz unit and one 100-MHz unit provide memory of 4k samples/channel. In the two-channel mode, all others provide 8k samples/channel. US prices range from $950 to $2290.

—by Dan Strassberg

▷**LeCroy Corp**, www.lecroy.com.

FEEDBACK LOOP

"The biggest problem with traffic lights is the people who set them. Locally, we have an advisory council who sets speed limits and traffic lights. The head of the group (a county employee) uses the excuse that he doesn't know how to set them to match traffic flow, but he's still employed and still setting them to impede traffic."

—Reader Robert Wethington, in *EDN*'s Feedback Loop, at www.edn.com/article/CA6590194. Add your comments.

DILBERT By Scott Adams

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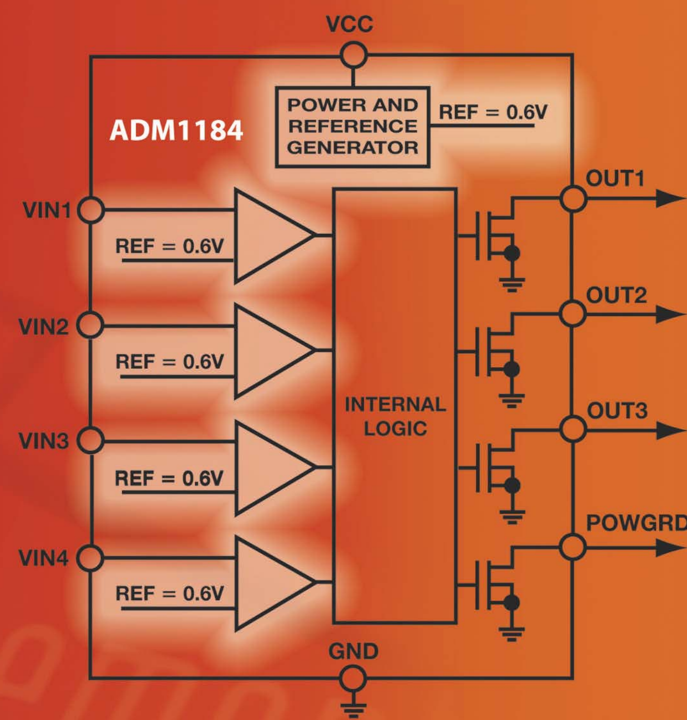

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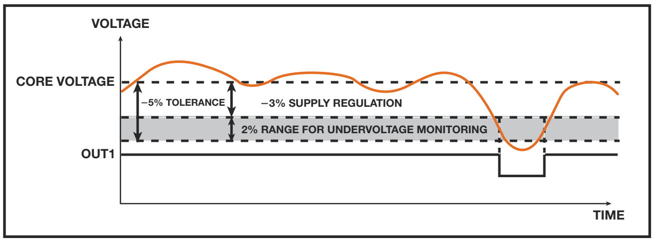

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ANALOG DEVICES

POE devices cater to higher-powered applications

Manufacturers of PDs (powered devices) that rely on the IEEE 802.3af POE (power-over-Ethernet) standard rather than ac wall power can shrink board space and the BOM (bill-of-materials) costs. They achieve this reduction by using a PD-interface-control IC to handle PWM (pulse-width-modulation) control for the PD's external-power-supply magnetics and switching devices, as well as network-interface chores. (For more on the emerging higher-powered POE standard and its nonstandard versions, see "Power-over-Ethernet chips: to the spec and beyond," this issue, pg 25, www.edn.com/081016df.)

Both the current IEEE 802.3af standard, which sets the load to the PD at 12.95W, and the draft 802.3at version, which sets the load power at 25W, require PDs and PSE (power-sourcing equipment) to perform network detection, classification, and UVLO (undervoltage lockout). Using these functions, the PSE and PD cooperate to determine the PD's power requirement and ensure that the PSE applies power only to POE-enabled equipment. The system controller at the central location can determine the overall power budget and, if necessary, allocate power during power failure from its available UPS (uninterruptible-power-supply) budget.

After a user plugs an Ethernet cable from a PSE into a PD, the PSE interrogates the PD to determine whether it is POE-enabled. This detection phase prevents the PSE from applying power to a non-PE device. The PSE applies a voltage ramp to the PD and looks for a 25-kΩ impedance. If the PSE sees an incorrect impedance, it knows that the device is not POE-capable, assumes a standard Ethernet connection, and applies no power. If the PSE detects the signature impedance, the PSE moves on to the classification phase. The signature-identification ramp voltage is 2.5 to 10V. A 24.9-kΩ resistor provides the correct signature impedance for detection.

As the PSE ramps the voltage to the PD, the PD must draw a specified current to identify the device class when the ramp is 15 to 20V. The amount of current the PD draws indicates its classification, which communicates the amount of power the PD will require during normal operation. The PSE sends this power information to the Ethernet-system controller, and the controller uses the information to determine its power budget. After the classification phase, the PSE continues to ramp up the input voltage to the operating voltage of 30V, after which the PSE releases the UVLO pin, and the PD powers up.

> "The PSE and PD cooperate to determine the PD's power requirement and ensure that the PSE applies power only to POE-enabled equipment.

All PD-interface-control ICs provide these network-interface functions. However, the ICs vary in the amount of power they can make available to the PD. In anticipation of the higher-power IEEE 802.3at POE version, On Semiconductor and Texas Instruments have introduced two POE-PD-interface controllers.

On Semiconductor's NCP1080 and NCP1081 PD controllers are both compatible with the 13W IEEE 802.3af. In addition, the 1081 is compatible with the 25W IEEE 802.3at, and it enables nonstandard devices with as much as 40W.

On Semi's newest POE-family members, the NCP1080 and the NCP1081 PD controllers, are both compatible with the 13W 802.3af standard, and the 1081 is compatible with the 25W 802.3at version. In addition, for designs requiring a proprietary higher-power scheme, the 1081 supports nonstandard extended, regulated power as high as 40W to the application load in a two-wire-pair power-supply configuration. This higher-power capability allows equipment manufacturers to offer higher-powered devices that comply with the POE standard in all respects except for power, making a straightforward route for designers to implement proprietary versions of POE.

The chips also feature 3-kV cable-ESD (electrostatic-discharge) protection, an important feature for applications that rely on extended Ethernet cabling outside a building. This scenario is typical of many surveillance-camera installations, for example.

The two devices are pin-compatible, allowing designers to start with the lower-power version and swap in the higher-power version as power needs increase. The NCP1080 and the NCP1081 are available in 4.4×6.5-mm TSSOP-EP20 packages and sell for $1.45 and $1.80 (1000), respectively.

TI's new, $1.65 (1000) TPS23754 PD-interface-controller IC, available in a 14-pin TSSOP, is IEEE 802.3at-draft-compatible and includes an efficient active-clamp-rectification circuit.

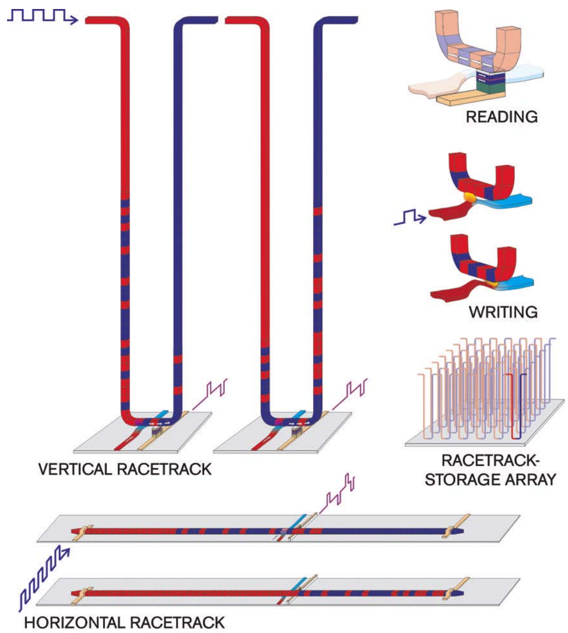
—by Margery Conner

▷**On Semiconductor**, www.onsemi.com.

▷**Texas Instruments**, www.ti.com.

RESEARCH UPDATE

BY MATTHEW MILLER AND ANN STEFFORA MUTSCHLER



"Racetrack" memory encodes data using oppositely magnetized regions in either horizontal or vertical arrays of nanowires.

IBM, ITRI explore solid-state "racetrack memory"

IBM Corp has started joint-development work with ITRI (Industrial Technology Research Institute) to explore the "racetrack-memory" approach to solid-state memory. IBM Fellow Stuart Parkin, PhD, conceived the idea at IBM's Almaden Research Center in San Jose, CA.

Developers of racetrack memory named it because data race around a nanowire "track." It promises a high-capacity, nonvolatile-storage device with high performance, high durability, and low energy consumption. The technology stores data in the form of "domain walls"—boundaries between regions of opposite magnetic polarity in the magnetic nanowires.

Each racetrack stores many domain walls, allowing high data density and low cost—as low as flash memory using horizontal racetracks and potentially as low as magnetic disk drives using vertical racetracks, according to IBM.

IBM has demonstrated that short pulses of spin-polarized current can controllably move several domain walls back and forth along a racetrack, the key underlying principle of this memory. IBM and ITRI believe that this technology could allow a handheld device, such as an MP3 player, to store approximately 500,000 songs or approximately 3500 movies—100 times more than is possible today—with far lower cost and power consumption.**—ASM**

▷**IBM**, www.ibm.com.

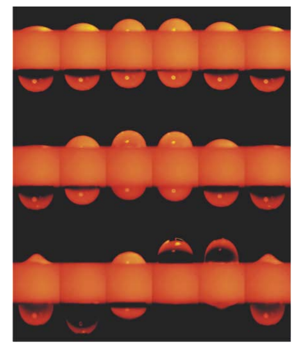
▷**Industrial Technology Research Institute**, www.itri.org.tw.

Tiny lens harnesses oscillating water droplets

From cell phones to military drones, many applications demand small, light optical lenses but can't spare much power for focusing them. Researchers at Rensselaer Polytechnic Institute claim to have developed an innovative liquid lens that fits the bill.

The lens features a pair of water droplets that oscillate when you expose them to high-frequency sound from a small speaker. The oscillations effectively move the lens into and out of focus, with respect to the scene being photographed, hundreds of times per second. By capturing 250 frames/sec and using image-processing software to discard out-of-focus frames, the system produces a stream of in-focus images.

Although other miniature-lens technologies have exploited water as a material, they have relied on time- and power-consuming physical manipulation of the shape of the lens to change focus (see "Licensing agreement advances tiny zoom lenses," *EDN*, Aug 16, 2007, www.edn.com/article/CA6466224). By eliminating the need for high voltage or an exotic activation mechanism, the new technology promises to outpace those competing technologies in power, weight, and speed, according to the researchers.**—MM**



High-frequency sound forces water droplets in a new lens to oscillate in this series of time-lapse photos.

▷**Rensselaer Polytechnic Institute**, www.rpi.edu.

SLIMMER LIGHT GUIDE HERALDS ULTRATHIN-LCD PANELS

Philips Research recently displayed a prototype of a 32-in. LCD television that measures only 8 mm thick–about 20% as thick as the slimmest commercially available panels. The key to the skinny design is a 1-mm-thick light-guide plate that uses patented technologies to uniformly distribute light from high-power, energy-efficient LED backlights. Light plates today measure approximately 25 mm deep and account for most of an LCD panel's overall thickness. The technology also reduces weight by as much as 10 kg (22 lbs) for a 32-in. television, according to the company, which has not disclosed a time line for commercial introduction.—MM

▶Philips Research, www.research.philips.com.

A prototype LCD television measures just 8 mm thick, thanks to a 1-mm-thick light-guide plate.

10.16.08

RAQ's

Rarely Asked Questions

Strange stories from the call logs of Analog Devices

Single Supply Amplifiers—They Sound Simple...are they?

Q. Running rail-to-rail op amps on a single supply sounds like a winning combination, but what drawbacks will I encounter when using amplifiers like this?

A. Single-supply and rail-to-rail outputs are a great combination, but there are a few parameters that warrant a second look. Your question doesn't specify whether you are talking about single-supply amplifiers (a particular class of amplifiers) or running a traditional op amp on single supply; we'll discuss both cases.

By definition, a true "single-supply" op amp operates on one supply, and the input common-mode voltage range of the amplifier includes the negative supply rail. Note that even though the input of the amplifier may be able to go to the negative rail and beyond it doesn't mean the output can. I'll say more about that when we talk about rail-to-rail outputs.

Any amplifier can be run on a single supply. Op amps don't have a ground pin and are equally happy when run on a bipolar supply as they are with a single supply. Additional bias circuitry is required when running an amplifier in this configuration, however. As a result, the amplifier's performance may suffer slightly in the following areas: lower bandwidth, degraded power supply rejection (PSR), and higher noise.

The term rail-to-rail output is a misnomer. While the amplifier output can get close to the supply rails, it never quite gets there. In bipolar amplifiers, the rail-to-rail output stage is typically a common emitter; therefore the closest the output can get to the rails is a saturated transistor drop Vcesat. The value of Vcesat is dependant on the amount of load current delivered by the amplifier. For low currents, the output can come to within tens of millivolts to the rail. For higher currents Vcesat can approach 0.5 V or more. Some new amplifiers now feature on-chip charge pumps to make up the Vcesat drop, allowing the output to truly swing all the way to the rail.

An amplifier output swinging close to the supply rail may appear fine when measured on an oscilloscope, but a network analyzer may reveal a different result. As the output swings closer to the rails, the output transistors no longer operate in the linear region. As a result, distortion is introduced. Distortion can occur several hundreds of millivolts away from the rails. Therefore when possible, try design in a little extra headroom from the rails; this will help improve the amplifier distortion performance.

We've only skimmed the surface on these topics. For in-depth application and product information, visit our website or click on the link below.

To Learn More About Single Supply Amplifiers
Go to: http://rbi.ims.ca/5726-101

Contributing Writer John Ardizzoni is an Application Engineer at Analog Devices in the High Speed Linear group. John has been with Analog Devices since 2002, he received his BSEE from Merrimack College in N. Andover, MA and has over 28 years experience in the electronics industry.

Have a question involving a perplexing or unusual analog problem? Submit your question to: raq@reedbusiness.com

For Analog Devices' Technical Support, Call 800-AnalogD

BY HOWARD JOHNSON, PhD

The shot heard 'round the world

Professor Wallace Clement Sabine removed a cheap, nickel-plated pistol from his waistcoat, raised the weapon above his head, and pulled the trigger. An earsplitting crack washed over the auditorium, penetrating every crevice. The sound reverberated wildly for eight full seconds, passing back and forth across the room some 50 times or more. As the echo slowly died out, the professor turned to face his audience. Wiggling a finger finger in one ear, he began to lecture, "There we have the impulse response of a Gothic cathedral."

The year was 1898, and Sabine was just developing his theory of acoustics—a theory that has since influenced the design of every great symphonic-performance hall. Sabine asserted that the most significant parameter is the reverberation time. He further stated that, with only two constants, you can predict in advance of construction the expected reverberation time.

The two constants you need are, first, the average fraction of acoustic power reflected at the boundaries of the room. Next, you must know the mean time required for acoustic waves to transit the structure.

For example, if the average attenuation coefficient for waves bouncing off the walls, ceiling, and floor is 2 dB, then it probably takes on average about 30 bounces for the sound to die down to a level 60 dB below the source. If the mean time between bounces (the mean transit time) is T, then the 60-dB reverberation time, RT_{60}, equals $30T$. In general, given a reflection coefficient, r, expressed in decibels, the 60-dB reverberation time equals $(60/r)T$. The remainder of Sabine's theory refines that basic idea with a little algebra.

> **The most significant parameter (in performance-hall design) is the reverberation time.**

Let's apply Sabine's theory to a digital problem. Assume a simple, unilinear transmission path. Sabine would define the time required for reverberant signals to damp down to a level x dB below the source signal level as $RT_x=(x/r)T$, where T is the round-trip delay, x is the required level of damping in units of decibels, and r is the round-trip attenuation coefficient in decibels. Coefficient r includes the sum of attenuation coefficients at either end of the transmission line plus the round-trip attenuation of the transmission line itself. In a highly reverberant system, the formula RT_x predicts how long you must wait after each data edge before the line settles to an acceptable degree.

In a hairball network with many interconnected nodes, the same theory applies but with a slightly different interpretation. Coefficient r represents the average attenuation at each discontinuity, and T becomes the average transit time between discontinuities.

Regardless of the topology, the expression for RT_x, because it contains three terms, supplies three basic ideas for improving signal quality:

- Reduce x. Single-ended logic with widely spaced V_{IH}/V_{IL} (high-input-voltage/low-input-voltage) thresholds typically requires damping of at least $x \geq 20$ dB. Differential logic, because it has tighter input-threshold specifications and thus larger percentage-voltage margins, can work with less damping. By analogy to the acoustic world, it is easy to design a building for listeners who do not require perfect acoustics, such as rock 'n' roll fans who don't mind massive reverberation.
- Increase r. Intentional terminations at one or both ends of a transmission line dramatically increase the round-trip attenuation. Sabine would advocate draping a large room with heavy curtains and using well-padded seats to damp reflections. Nowadays, large buildings incorporate acoustic ceiling tiles and thick carpet.
- Decrease T. Shrink the line length or change the dielectric constant. Lowering the dielectric constant slightly speeds signal propagation, decreasing T. Both ideas help. Acoustically, Sabine's equation teaches that large rooms are more difficult to control and that a large room constructed at the top of Mount Everest would be the most difficult of all due to the low temperatures and thus relatively low speed of acoustic propagation.

Come to think of it, if I decide to build a symphony hall at the top of Mount Everest, just shoot me. EDN

Howard Johnson, PhD, of Signal Consulting, frequently conducts technical workshops for digital engineers at Oxford University and other sites worldwide. Visit his Web site at www.sigcon.com or e-mail him at howie03@sigcon.com.

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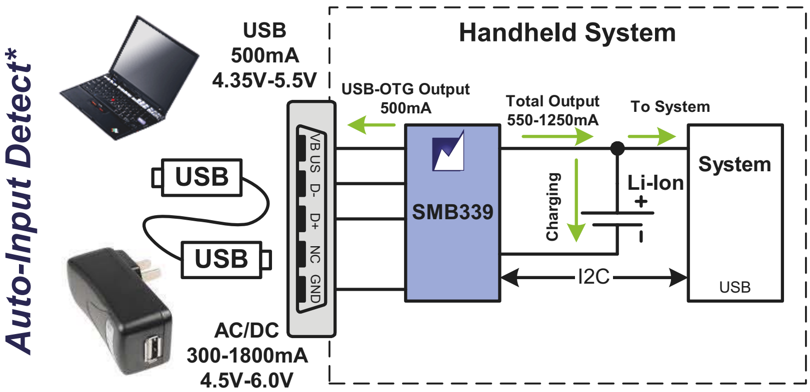

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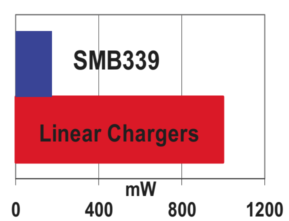

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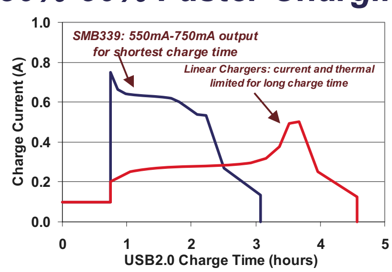

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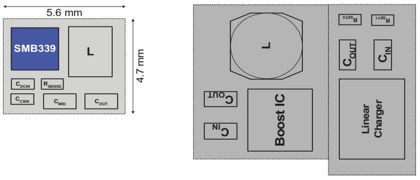

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Topology	Switch-mode	Switch-mode	Switch-mode	Linear-mode	Linear-mode
Input Voltage Range (V)*	4.35 to 6.2 (18)	4.35 to 5.5 (16)	4.35 to 6.5 (10)	4.35 to 6.5 (10)	4.35 to 6.5 (10)
# of Inputs/Outputs	1/1	2/2	1/1	1/1	1/1
Maximum Charge Current (mA)	1250	1500	900	525	210
TurboCharge™ Output	Automatic	Automatic	Software/uC	N/A	N/A
CurrentPath™ Control		X			
USB On-The-Go Power	X	X			
Low-Battery Recovery Mode		X			
I2C Interface	X	X	X	X	X
Programmable Float Voltage	X	X	X	X	X
Programmable Charge/Term. Current	X	X	X	X	X
Programmable Input Current Limit	X	X			
Input/Battery OV/UV	X	X	X	X	X
Hardware Safety Timer	X	X	X	X	X
Software Watchdog Timer	X	X			
Battery Thermal Protection	X	X	X	X	X
Automatic Input Current Limit	X				
Automatic Power Source Detection **	X				
IC Thermal Protection	X	X	X	X	X
Package	CSP-20	CSP-30	CSP-15 5x5 QFN-32	CSP-8	CSP-15

* () Indicates overvoltage "holdoff" tolerance
** Per USB Battery Charging Specification 1.0

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POWER OVER ETHERNET ALLOWS A BASIC CATEGORY 5 OR 6 CABLE TO CARRY BOTH DATA AND POWER, ENABLING SIMPLE AND INEXPENSIVE INSTALLATIONS OF EQUIPMENT SUCH AS VOIP PHONES, CAMERAS, AND WIRELESS-ACCESS POINTS.

BY MARGERY CONNER • TECHNICAL EDITOR

POWER-OVER-ETHERNET CHIPS: TO THE SPEC AND BEYOND

The benefits to end users of the IEEE 802.3af/t POE (power-over-Ethernet) standard are clear: Without relying on an electrician, anyone who can string a Category 5 or 6 cable can inexpensively install both power and data ports for networked applications in locations with no ac-power plug. Users can simply add a POE power supply at a typical price of $39.95 in a network-equipment closet and connect it with Category 5 twisted-pair cable. Contrast this scenario with the cost for a new power plug—as much as $2000, including labor and parts costs—along with the time you waste in scheduling an electrician's time.

A POE network has two main components: PSE (power-sourcing equipment), such as the network switch or central router, and PDs (powered devices), such as a VOIP (voice-over-Internet Protocol) phone or a wireless-access point, which connect to the network that delivers both power and data. Networks with a non-POE switch can still take advantage of POE by adding a midspan power supply, which injects power into the network independently of the switch or router, such as the enabling power supply in a network-equipment closet. Backing up the PSE with a UPS (uninterruptible power supply) ensures that your networked equipment, including VOIP phones, will continue to operate even if your office experiences a power failure.

VOIP phones and wireless-access points consume relatively little power. With these types of applications in mind, framers of the current POE IEEE standard, IEEE 802.3af, set the power limits for PDs at 12.95W. However, 13W is insufficient power for many types of equipment, such as multiport wireless-access points and PZT (pan-zoom-tilt) videocameras in building security and surveillance. The standards committee began work on a second version, 802.3at, or POE Plus. This version, currently in

AT A GLANCE

- POE (power-over-Ethernet) devices can reduce costs by combining data and power in a Category 5 or 6 cable, requiring no expensive power installation.
- The current POE standard, IEEE 802.3af, limits the power a device can draw to 12.95W, with a draft version, 802.3at, upping the limit to 25W.
- Try to keep application-power needs at less than 25W, but you can go nonstandard for applications with higher-power needs.
- Once the network goes outdoors, pay extra attention to surge protection.

draft form, increases the maximum power the PD can draw to 25W. Semiconductor vendors have introduced a bevy of POE ICs based on the draft version, aimed at enabling higher-power POE PDs (**Figure 1**). (Also see "POE devices cater to higher-powered applications," this issue, pg 18.) However, 25W is still not enough for some applications, which can require power well in excess of 30W.

The IEEE 802.3at standards committee started with a limit of 30W before lowering it to 25W because of test data that showed that Category 5 or 6 cable temperature increased significantly when installers buried it in a larger bundle of cables and it was carrying as much as 750 mA of current. The committee's concern was not about safety, because the possibility of fire in this case isn't even remote, but rather that the signal quality of the Category 5 and 6 cables begins to degrade when cable temperature exceeds 60°C.

However, the cables for applications that require higher power are often not in a large bundles. For example, PZT security cameras, with features such as cold-weather heaters, IR (infrared) lamps, and steerable microphones, are often outdoors and have dedicated cabling. Designers of systems for these applications may consider using a nonstandard version of POE, in which they follow all 802.3at parameters except for maximum PD power draw. With an eye toward these nonstandard applications, all of the POE-interface ICs for the POE Plus version can support more than 25W of power.

Deviating from an industry standard can be a daunting move, but if your PD requires more than 25W, you may have no choice. You can take steps, however, to lower the risks associated with nonconformity. First, ensure that your device's design really requires more than 25W. PDs of the past share a trait common to almost all electronics that emerged before the current surge in energy prices: inefficiency in their use of energy. Power supplies of five to 10 years ago were often only 80% or less efficient. You should now be able to buy or design a power supply with more than 90% efficiency, which may be enough additional power that your design won't need more than the standard's 25W limit.

If your PD has an efficient power supply and still requires more than 25W, however, you may next want to consider the network cabling. Will your application have to work with minimum standard cabling? If so, you must allow for fairly high losses in the cabling system. If, on the other hand, you can specify the cable for your equipment, you

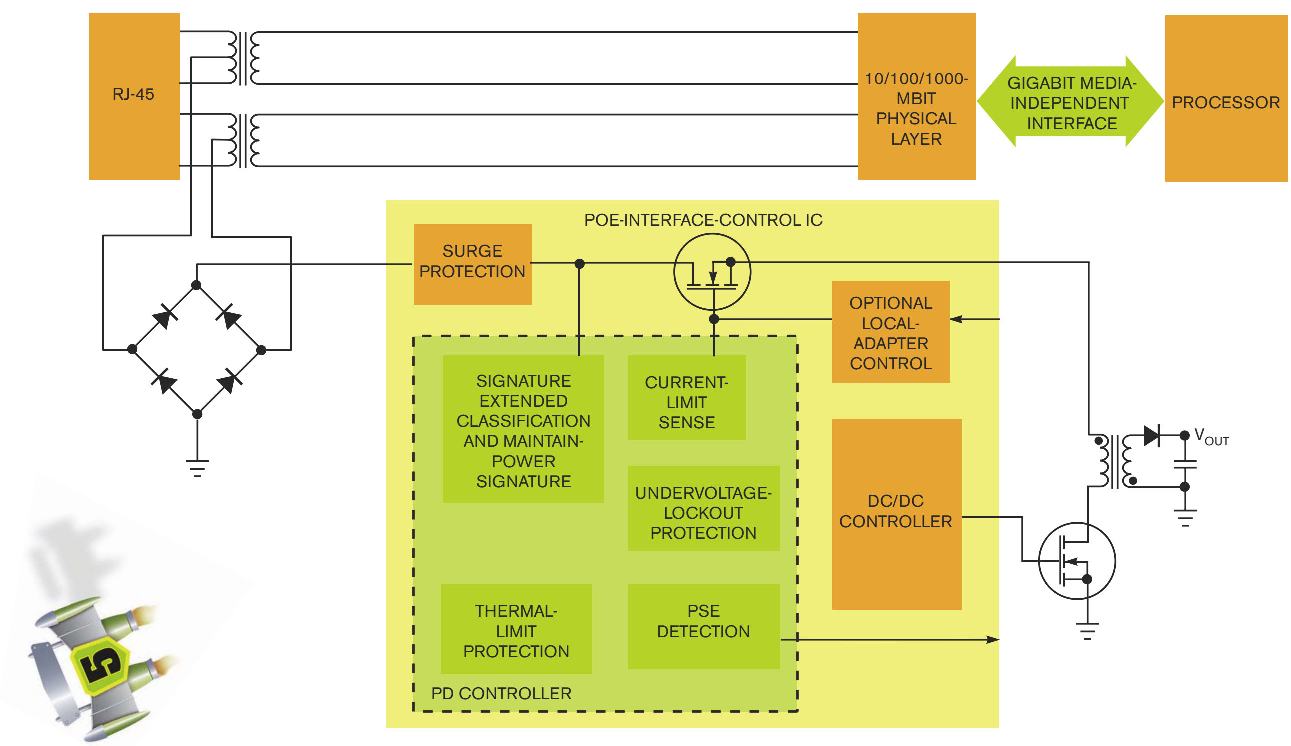

Figure 1 POE-PD-interface chips handle the IEEE 802.3 interface chores, including detection, classification, and undervoltage lockout, and they provide dc/dc control for the PD's voltage converter.

Power That Gives You The Best Of Both Technology Worlds

Switcher Efficiency Combined With LDO Noise And Transient Performance

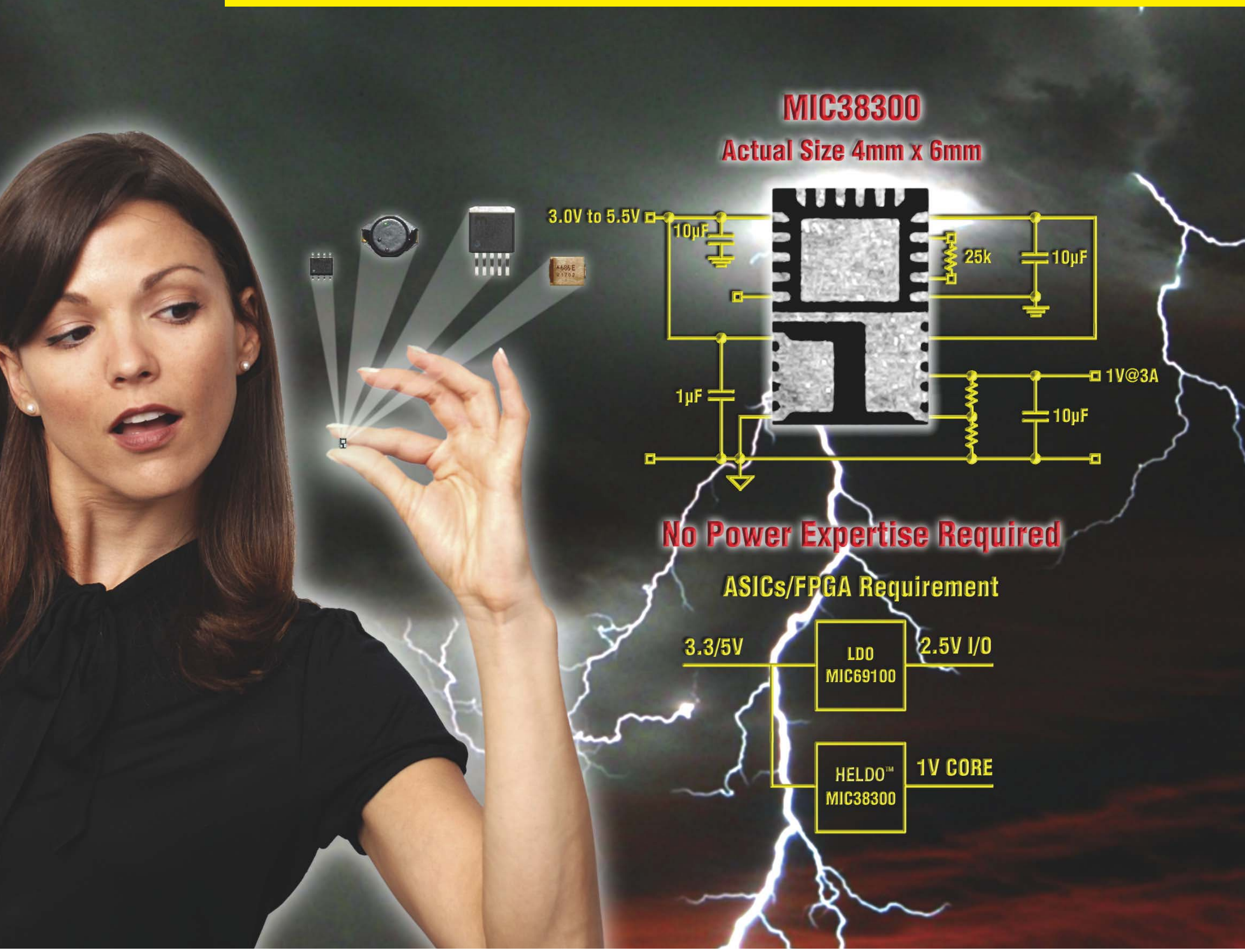

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Figure 2 Legacy Ethernet systems can include POE capability with the addition of a midspan power supply that injects a POE voltage into the network. The single-port POE 60U-560G from Phihong provides 60W and costs $62 (one).

can go from Category 5 to Category 6, which generally has a higher wire diameter and correspondingly less resistance and wasted power.

"Over time, the cable will degrade as it carries more power because Ethernet cables are not really power-delivery cables," says Mike McCormick, manager of Texas Instruments' POE-products group. "They're not solid-core cables; their primary use is for signal transmission. So, when we use them for power, they're not the best conductor. You have to be aware of what type of cabling your customer will use—certainly if you're going to something that's beyond the standard. If your device is nonstandard, it may not make sense to stay with standard cabling."

Make sure you get buy-in from your marketing department, which is often the entity that sets parameters such as going with a nonstandard and therefore more expensive cable. "I've met with customers who were designing outside installations of cable, and their marketing department says, 'No, we have to work with the most generic cable standards,'" says McCormick. However, there is no large installed base of outdoor data-communications customer-premises wiring. Limiting your product to "standard" cabling that's for a different environment may not make sense.

Another option and one that the POE standard allows is to use four pairs rather than just two pairs. Keith Hopwood, vice president of marketing for Phihong Power, maker of midspan-power supplies (**Figure 2**), says that, although he has heard anecdotally of a few European installations that used two-pair cable, he has never encountered any installation that didn't use four-pair cabling. Using four pairs increases the amount of power available at the PD and minimizes the heat in the cable. At some point, if cabling and installation costs become significant, you need to evaluate whether bringing in an ac plug might be the best approach.

The issue of resistive-cable losses can also be a surprise with nonstandard installations because the standard's guarantee of available power at the PD no longer shelters your design. The standard guarantees 13W to every PD, and it

+ For more on POE's move beyond videocameras and VOIP phones for the factory floor, go to www.edn.com/blog/1470000147/post/210031021.html.

+ For an article on POE controllers' gearing up for a new physical layer, visit www.edn.com/article/CA6543804.

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also limits the cable run to 100m. Once you go nonstandard, you must calculate the power and voltage drop the cable incurs and determine the power that will be available at the PD.

If you're designing PSE capability into a switch for compliant or noncompliant systems, you must ensure that the switch actually uses the power it allocates for PDs. Harmik Singh, business-development manager for Maxim's POE products, emphasizes the importance of power budgeting for PSEs. "Power is scarce, and you don't want to allocate more than the PD is actually consuming," he says. If a PD identifies itself as a POE Plus type of device that will require 25W or more but consumes only 10W, the PSE should be able to determine that situation so that it doesn't allocate the unused power. For example, Maxim's MAX5952 PSE-controller IC measures the actual current that the PD is consuming, digitizing and reporting in real time the PD's power consumption so that the system controller can allocate the actual power usage.

With all of the concerns that can arise with noncompliant POE installations, it's worth asking: Why not have a flavor of the specification that accommodates higher-power devices? TI's McCormick provides an answer: "In the networking world, it has held true that every option eventually becomes a requirement," he says. A 96-port switch that must supply 50W/port is a more complex and expensive design than one that must provide 25W/port, especially because the number of high-power PDs on the market, although significant, will probably not dominate the market. For example, an eight-port router, with each port providing 50W, would burden the router with 400W, which most applications would not use.

Even as POE makes Ethernet increasingly attractive within offices and factories, its power-and-data combination also makes it attractive in exterior applications, such as security cameras and sensor networks. However, once electronic communication systems go outdoors, their susceptibility to power surges increases dramatically. Lightning strikes are the most likely cause of a catastrophic surge, but other random events can also send a debilitating surge through the network. The Ethernet cable serves as an antenna, picking up virtually any

> "IN THE NETWORKING WORLD, IT HAS HELD TRUE THAT EVERY OPTION EVENTUALLY BECOMES A REQUIREMENT."

surge, discharge, or transient.

PD-interface-controller ICs come with a variety of protection schemes. TI's family comes with minimal internal protection, assuming that designers will want to tailor their designs to the end applications. "When it comes to voltage suppressors and diodes, we believe you're better off going to a [protection-device vendor]," says McCormick. You can get a higher voltage rating, he notes, and the devices can handle much more power than a mixed-signal device.

Other IC vendors offer integrated surge protection. For example, On Semiconductor's NCP108X POE-PD-interface controller provides 3-kV cable-ESD (electrostatic-discharge) protection because the company fabricates the device on an automotive-qualified, high-voltage process. Akros Silicon's AS1135 PD controller offers over 16.5-kV air discharge, 8-kV contact discharge, and 6-kV surge on-chip protection, with a low impedance path to ground. **EDN**

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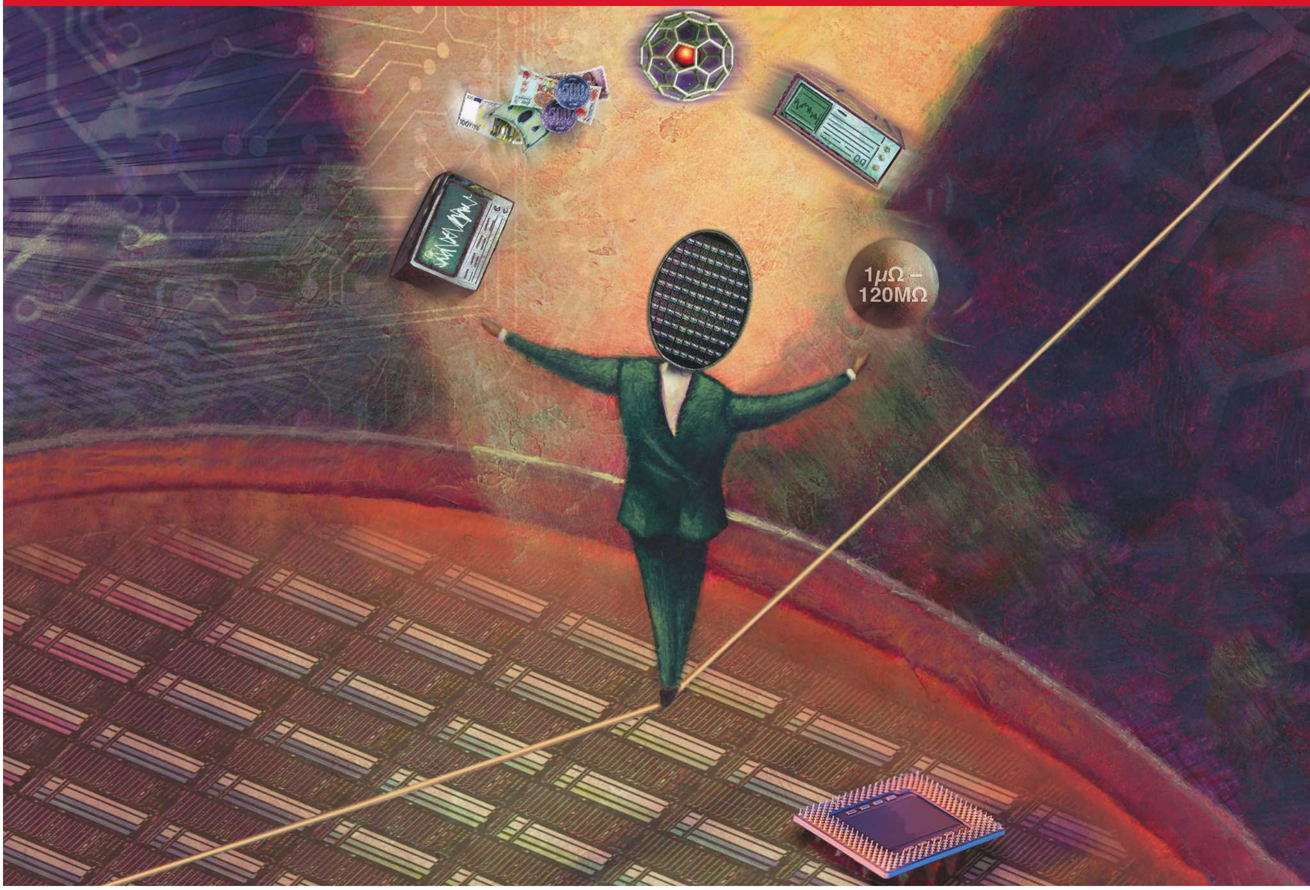

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BY RON WILSON • EXECUTIVE EDITOR

A TURN-OFF

Power management complicates life for verification engineers

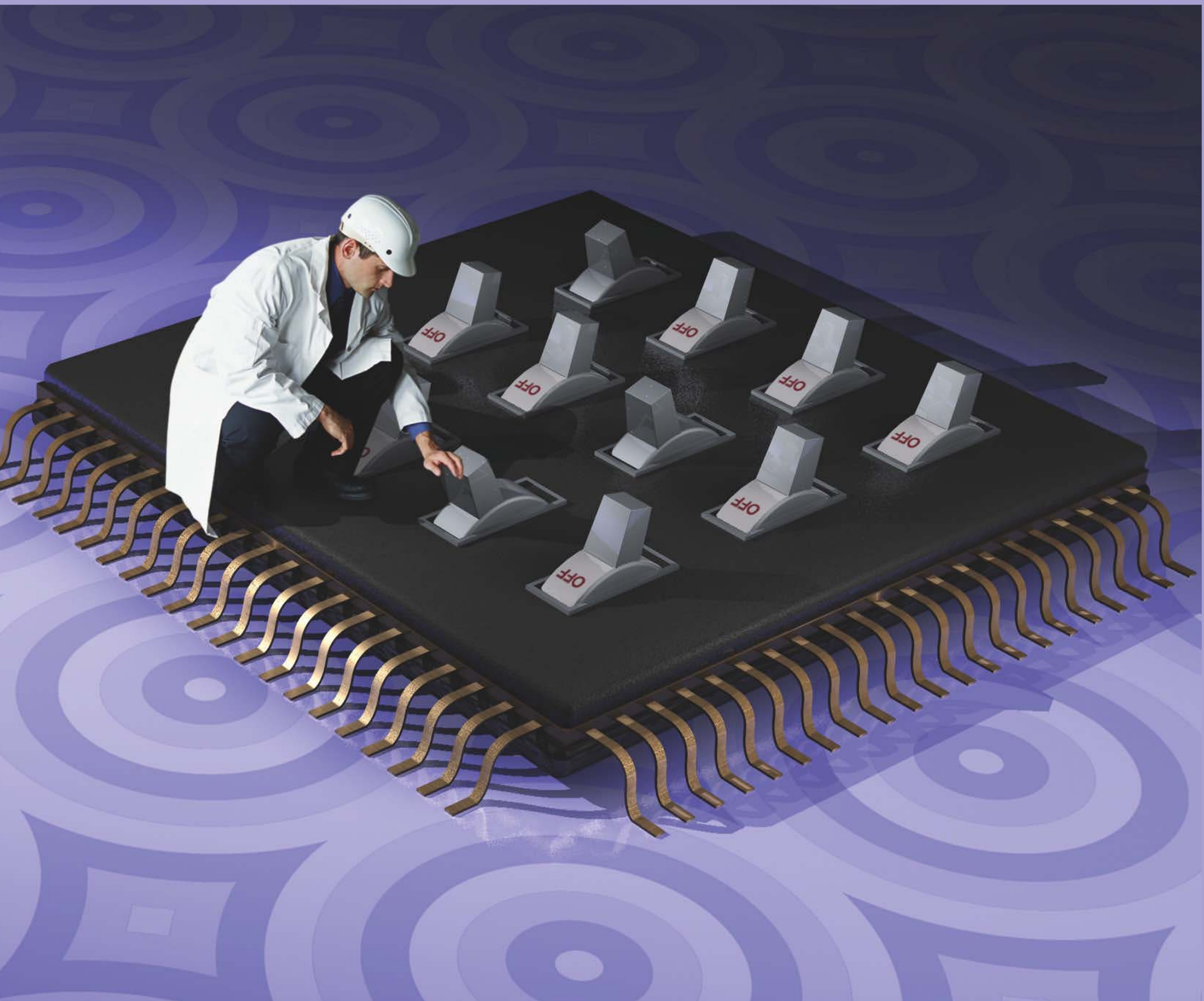
ADVANCED ENERGY-SAVING TECHNIQUES CAN CAUSE VAST DIFFICULTIES IN THE VERIFICATION PROCESS.

There is intense pressure on all levels of chip engineering to reduce power consumption. That situation, in turn, has led to increasingly dramatic—and invasive—measures to reduce power in individual blocks and circuits.

These efforts have been extremely successful, but they have come at a cost in design complexity—often the topic of conferences. At least as serious, and much less discussed, there has been a serious impact on the verification process. At best, aggressive power management complicates functional verification. At worst, it can render a design unverifiable. *EDN* has spoken with design teams in the United States, Europe, and Asia to understand the scope of the problem in logic design and to see how the best designers are coping with the new verification challenge.

The most used logic-level power-management techniques fall nicely into a few categories, based on the obvious ways to reduce static and dynamic power. For static-power reduction, the only simple things you can do are to use high-threshold-voltage transistors as much as possible, reduce the voltage on the supply pins, or turn the supply off altogether. The techniques for accomplishing these tasks include multithreshold design, multivoltage design, and power gating.

For reducing dynamic power, your options are to reduce the supply voltage or reduce the frequency. Techniques for this process include clock gating and DVFS (dynamic-voltage-



frequency scaling). The **sidebar** "The one-minute power manager: a primer" contains a brief description of each of these techniques. This article will examine the impact of each of these ideas on verification.

CLOCK GATING

At a coarse level, clock gating can be one of the simplest techniques for reducing dynamic power. Hence, it sees frequent use in cases in which the main problem is to limit peak dynamic power. "We use mainly clock gating today … to limit package cost," says Laurent Ducousso, STMicroelectronics' IP (intellectual-property)-verification and system-modeling manager.

Ducousso says that his company's design teams define clock domains early, basing them on IP or subsystem boundaries. That approach allows the team to determine when a domain may be clock-gated based on a high-level view of the operating modes and to check the sequencing of clock gating as an added task in functional verification. The physical-design team inserts the gating circuitry during the back-end flow. In simple cases, clock gating does not impact the state within the block, so there is no need to verify state retention. But this case does not hold true for every block. "We are just getting into situations where we have to worry about state retention," Ducousso says. "We are looking at our test benches to see what we can do with verifying these situations. Assertions may turn out to be quite useful."

Functional verification of clock gating is just added work, not a new concept, according to Michael Floyd, IBM's chief architect for energy management in its Power Systems Group. "Basically, clock gating adds to the state space," Floyd says. "It needs to be timed and verified and tested in manufacturing like any other function." For improved test coverage, designers sometimes put in modes to disable clock gating. "But some designs use the clock gate as a hold tap on latches," Floyd comments, "so it becomes a part of the functional design, and we have to verify and test that function with clock gating turned on."

As clock gating gets more complex, the verification team's attention seems to shift from functional correctness to timing and signal-integrity issues. "We rely on design guidelines to get clock-gating structures functionally correct during the front-end-design process," explains Krish Krishnamoorthy, director of advanced methodology in the System LSI group at Toshiba. "Then, we check during physical verification to make sure everything came out right." These checks might include careful timing because, for instance, a late-arriving gate signal could gate a clock off during its active phase, with disastrous results downstream.

The complexity of this process varies. "For simple datapaths, there's hardly any impact on the verification process," says IBM fellow Brad McCredie. "But, if designers start using fine-grained clock gating in control logic, that's a major whammo to the verification process."

POWER GATING

Early in the pursuit of power management, design teams began to use voltage islands—separating blocks that did not have to run at the maximum clock speed and supplying them with reduced voltage. This practice imposed two new tasks on verification. First, it required that the verification team make sure that correct level shifters were in place on all of the signals passing between voltage islands, including clocks. Second, it required that cell libraries had timing files for each of the voltages at

AT A GLANCE

- Increasingly aggressive power management can mean trouble for verification.
- Each power-management technique creates its own verification issues.
- EDA tools today do not automate the verification process.
- A systems approach is necessary in both creating and verifying power-management structures.

which a design might use the cells and that the timing team used the right delays for the voltage at which a voltage island was operating. There are other issues, as well, when signals from one voltage domain cross another domain.

Once designers had declared and isolated voltage islands, it was a natural step to simply turn off the power to a voltage island when it was not in use. But this idea—power gating—creates a whole new set of issues for the verification team. Obviously, blocks that remain on must function correctly when power-gated blocks are off. Less obviously, turning the power off and on requires a delicate dance involving isolating the inputs and outputs, saving the internal state of the block, shutting off power, restoring power, restoring state, and reconnecting the block to the rest of the design (**Figure 1**).

"We verify power-gated designs in four stages," explains Freescale Semiconductor's senior director of engineering, Prashant Bhargava. "We examine the shut-off sequences. Then, we verify the design with the blocks in the power-off state, mainly to make sure they are properly isolated and have retained state correctly. Next, we verify the power-up sequences. And, finally, we verify the blocks in their power-on state."

Freescale, like many other companies, relies on Cadence CPF (Common Power Format) files to capture the intent of the power management. "In the CPF file, we identify the gating signals, what blocks are gated, the power controller, the interfaces between switched and unswitched blocks, the commands to isolate blocks, and the location of level shifters," Bhargava says. The CPF file becomes the central definition of design intent for power management and can drive some other tools—primarily, Cadence tools—downstream to direct such tasks as simulation and synthesis.

The CPF file may hold promise for centralizing the power design, but it also has its own significant issues. For example, there is no method for automatically checking the CPF file. "We can identify errors in the CPF only during the verification process," Bhargava explains.

Sam Leung, director of digital design at Staccato Communications, seconds this point. "Verifying that what you got out of synthesis is what you asked for is still a very manual, visual process," he says. In power gating in particular, the verification team has to manually check that the correct structures actually exist in the design. "There are so many inputs and outputs and so much manual table entry involved that errors happen," Leung says. "You have to check the files."

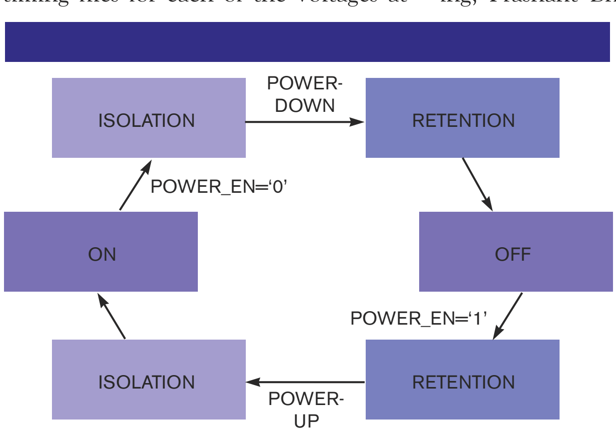


Figure 1 Power gating requires an orderly sequence of states to take a block into and out of power-down mode.

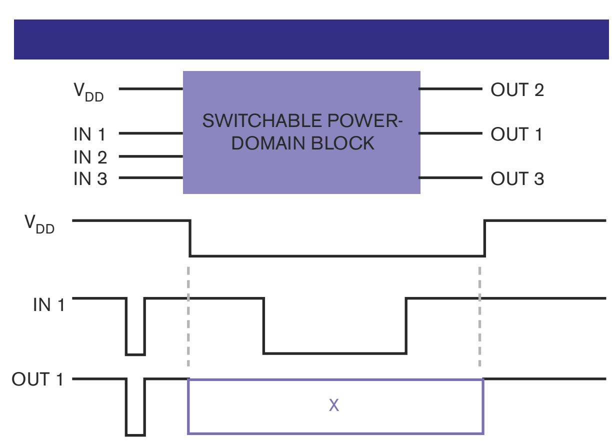


Figure 2 Power gating can generate unknown states in the functional simulation of a block.

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After verifying the CPF or UPF (Unified Power Format) files, there is the matter of verifying the design. "There is no tool to grab data out of the CPF file and generate a test bench for the power management," Leung laments. "We have to create a set of test vectors just to verify the operation of the power-management functions and the power controller. Today, we can perform these checks only at the functional level, not the gate level. The reason for this [situation] is that the big challenges come in checking signals that cross power domains," Leung explains. "You need to know if something is leaking somewhere. You can't verify these signals in isolation; you have to work with the full-system models."

Nilesh Ranpura, a design manager at eInfochips, also relies on CPF to organize the verification effort. "When you start verification, you have to understand which blocks are at which voltages," Ranpura says. In other words, he adds, "you have to identify the sequences of the power-control state machine and what the voltage combinations will be in each state. This [task] isn't automated, and the CPF data isn't accessible to all simulation tools, but, even so, we have found that having the CPF data has reduced our verification time by about 40%."

One of the problems Ranpura identifies is that, when you are turning power on and off in blocks, the signal states in the system are no longer limited to the simple 1, 0, X, Z, and so forth that most simulation tools offer. There are other possibilities. "If you use Boolean assertions, you sometimes have to suppress incorrect firings," Ranpura says.

IBM's Floyd agrees about the need for states beyond 1, 0, X, and Z in simulation (**Figure 2**). "When we initially started using power gating, it caused some indigestion because it increased the number of situations in which you deal with an unknown state," he says. "But it turns out that conventional X-state analysis is too pessimistic; removing all the X states hurts the critical paths. So, we are actively developing alternatives. In principle, a formal tool can verify that a power-gated domain could not corrupt data. That [ability] is exciting."

GROWING COMPLEXITY

Once the verification team is comfortable that the sequencer is in fact following the design intent, you must verify not only that the signal is arriving, but also that it is arriving at the correct voltage and on time. "When you are switching blocks that are connected to each other, you have to verify that the level-shifter sequencing is correct," says Ranpura. "It must exactly match the design intent, or you can generate huge numbers of errors with no easy way to trace them back to the problem."

Other non-Boolean problems arise, as well. "Memory blocks are an interesting issue for power gating," says NXP's microcontroller-design manager, Avindt Chopra. "You can power-gate them, but, if you do, you had better simulate the transitions very carefully—for instance, modeling the inrush current in the memory block as you change voltage."

Buses can be another important point to watch. "When you are gating an entire IP block," says ST's Ducousso, "if the block is connected to a system bus, you have to be certain that the bus interface stays electrically clean during the transitions." Ducousso makes another interesting point with regard to buses: Misfortune follows if you power down a block that has pending bus requests. In this case and probably in a good many others, the actual state that you must inspect before powering down the system may not reside fully inside the block. Some of it may be in an adjoining block that handshakes with this one, or it may be halfway across the chip in a bus arbiter. Another important case to check is the state of DRAM controllers during power sequencing. Corrupted memory from a spurious write cycle generated during a power transition can be nearly impossible to trace.

When a design moves from power gating to DVFS, things can get even more complex. "The complexity of a DVFS design completely explodes in verification," says NXP's Chopra. Now, every possible combination of voltages in the voltage islands in the system represents a new corner that you must examine.

Fortunately, the steps are about the same. First, verify that the power sequencer is doing what the designers intended. Now, this problem is more complex, however, because it involves the application software as well as the hardware. In DVFS, you may change the voltage on a block because the software

THE ONE-MINUTE POWER MANAGER: A PRIMER

As energy-conservation requirements have grown more stringent, many techniques have emerged for saving active and leakage power in logic circuits. It is not uncommon to find multiple techniques at use in different parts of a design. Here is a quick overview of these approaches.

CLOCK GATING

Clock gating is one of the earliest techniques for reducing dynamic power. It can increase static power because the clock-gating cells need to be fast, and designers often implement them with large, low-threshold transistors. This method simply shuts off the clock to portions of the circuit that are inactive.

Originally, designers used clock gating at the block level as a way of creating a standby mode. More recently, designers have employed fine-grained clock gating, down to the level of individual latches. Control circuitry can simply decide not to issue a clock pulse on a cycle when the data in a latch does not change. "We see designers using clock gating as a 'hold' tap on latches," says Michael Floyd, IBM's chief architect for energy management in its power-systems group. Thus, fine-grained clock-gating schemes can become exceedingly complex.

VOLTAGE ISLANDS

If some blocks can be slower than others, it makes sense to run the slower blocks at a lower frequency and turn down the supply voltage until these blocks just meet timing. This technique was also one of the early approaches–slightly more complex than coarse clock gating, especially in its impact on timing closure.

POWER GATING

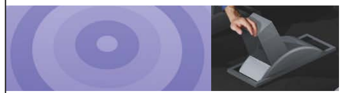
Power gating involves turning off the supply voltage to a block to stop both static- and dynamic-power consumption. The technique is more complex than it sounds. You have to be sure that there will be no activity needed from the block when the power is off. You also have to deal with state–including whether to preserve state while the power is off, where to save it, and how to restore it. It may also involve determining how to sequence the shutdown and power-up cycles and whether you can anticipate activity on the block early enough to perform the power-up sequence. You also must isolate the block from surrounding circuitry during power transitions.

DVFS

DVFS (dynamic-voltage-frequency scaling) is a blend of voltage islands and power gating: You adjust the voltage and clock frequency of each block on the fly so that it is just meeting its deadlines for the current task. This approach requires the ability to modulate clocks on a block-by-block basis, to dynamically vary supply voltages at the same granularity, and to ensure that nothing unexpected will happen while you are switching to a new operating point. It requires fairly detailed knowledge of the application's performance requirements. And the whole chip must meet timing at every legal combination of block operating frequencies.

DTVC

In DTVC (dynamic-threshold-voltage control), you dynamically control the threshold voltage on individual sets of transistors, thereby choosing a leakage-versus-speed point that just matches the requirements of the moment on a path. This approach is effective, but it requires special structures in the semiconductor process. It is custom-design stuff today, primarily in use by only a few advanced-processor vendors.



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says the block doesn't need to be fast for its current task. In fact, in DVFS designs, sequencing becomes so complex that designers often opt for a microcontroller or a task on a CPU in place of a state machine. This situation makes sequence verification a software-verification problem as well as a hardware-verification challenge.

Next, it is necessary to verify that the blocks in isolation are going through the correct sequence of events on voltage changes. This process can become nightmarishly complex because the sequencer, clock-gating circuitry, state-retention circuitry, and isolation buffers may all be in different voltage and clock domains and hence subject to different timing. "We have seen clock-gating signals released prematurely because of differences in voltage levels that were not captured by the simulator, for instance," eInfochips' Ranpura relates.

IBM's Floyd points out that, when connected blocks are working at different voltages and frequencies, the system has in effect become globally asynchronous and locally synchronous. "We have developed tools to detect asynchronous paths and to check their attributes when they cross a synchronous domain," Floyd explains. "For instance, we might modulate the cycle time on a clock to verify that there will be no loss of data. And we audit designs to make sure that domain crossings comply [with] one of a few acceptable techniques."

Signal integrity can be an issue, as well. "It is not just a matter of ensuring correct functional behavior at all the new combinations of corners," warns Toshiba's Krishnamoorthy. "Remember that crosstalk can be different depending on voltage." So, for instance, a signal might not be an aggressor when the block in which it is originating is at low voltage. It might become a serious problem, however, if the originating block is running at high voltage and frequency and the signal crosses a block that is turned down.

A SYSTEMS APPROACH

The details of what you need to check during verification of a power-managed design seem endless. But one thing many experts emphasize is that you must verify the design as a system, not as blocks in isolation. Many of the key issues, particularly in power-gated and DVFS designs, which can have many signal levels and asynchronous clock domains, occur not within blocks but between blocks. Thus, it becomes necessary for the verification team to examine the interactions between blocks at different combinations of power and frequency.

Emerging tools such as CPF and UPF can help keep track of these complexities on a full-chip level, but they are neither universally compatible with widely used tools nor universally used among design teams. IBM, for example, has its own internal tools for domain tagging and tag inspection during verification to keep the power state of the system known and consistent.

Even at the architectural level, power management is imposing changes to make verification more viable. "We have logical design hierarchy based on functional blocks, and we have physical hierarchy based on the implementation," observes Rob Cosaro, systems/architecture/applications manager of business-line standard ICs and microcontrollers at NXP. "But, increasingly, we have a third hierarchy based on clock and voltage domains. Power management in effect is defining another hierarchy." And having that hierarchy clear from architectural design may be the most important factor in making verification successful.EDN

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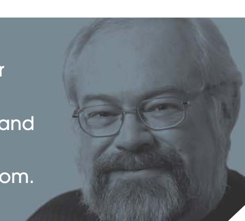

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Start with the right op amp when driving SAR ADCs

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For optimum SAR-ADC performance, the recommended driving circuit is an op amp in combination with an RC filter (**Figure 1**). Although this circuit commonly drives ADCs, it has the potential to create circuit-performance limitations. If you don't properly select the input resistor, R_{IN}, and the input capacitor, C_{IN}, values, the circuit could produce ADC errors. Worse yet, it could cause the amplifier to become unstable. If you ignore the op-amp open-loop output impedance and UGBW (unity-gain bandwidth), you may run into amplifier-stability issues.

The optimized ADC-driver circuit in **Figure 1** uses an op amp to separate the ADC from high-impedance signal sources. The following RC lowpass filter, R_{IN} and C_{IN}, performs functions going back to the op amp and forward to the ADC. R_{IN} keeps the amplifier stable by "isolating" the amplifier's output stage from the capacitive load, C_{IN}. C_{IN} provides a nearly perfect input source to the ADC. This input source tracks the voltage of the input signal and charges the ADC's input sampling capacitor, C_{SH}, during the converter's acquisition time.

In evaluating the circuit in **Figure 1**, you can determine the guidelines and constraints for selecting the value of R_{IN}. The op amp's open-loop output resistance, R_O, and the UGBW or the unity crossover frequency, f_U, as well as the value of C_{IN}, govern this issue (**Reference 1** and **Figure 2**). After defining the design formulas for R_{IN}, you can determine the value of C_{IN}. The ADC's acquisition time and input sample-and-hold capacitance, C_{SH}, as well as R_{IN}, influence the value of C_{IN}.

Once you understand how this circuit operates, you can establish the criteria for a stable system and define an appropriate design strategy. A proof of concept uses two sample circuits. The first is relatively stable; the second is marginally stable.

OP-AMP STABILITY WITH R_{IN} AND C_{IN}

The ADC in **Figure 1** cycles through two stages while converting the input signal to a digital representation. Initially, the converter must acquire the input signal. After acquiring the signal, the converter changes the sampled information, or "snapshot," of the input signal to a digital representation. A critical part of this process is to obtain an accurate snapshot of the input signal. If this ADC-data-conversion process is to run smoothly, the driving amplifier must charge the input capacitor to the proper value and maintain stability during the ADC's acquisition time.

You can determine the stability of an amplifier with a Bode plot, a tool that helps you approximate the magnitude of an amplifier's open- and closed-loop-gain transfer functions. In **Figure 2**, the units along the Y axis describe the gain in decibels of the amplifier in **Figure 1**. The units along the X axis describe the frequency in log, hertz of the open- and closed-loop-gain curves.

If the closure rate of the closed- and open-loop-gain curves

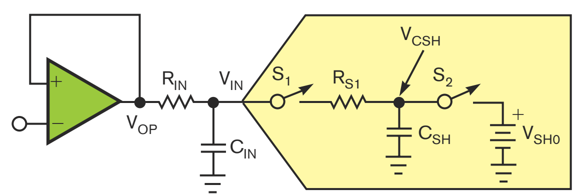

Figure 1 In this circuit, R_{IN} "isolates" C_{IN} from the op-amp output stage. C_{IN} provides a charge reservoir for the SAR ADC during the sampling period.

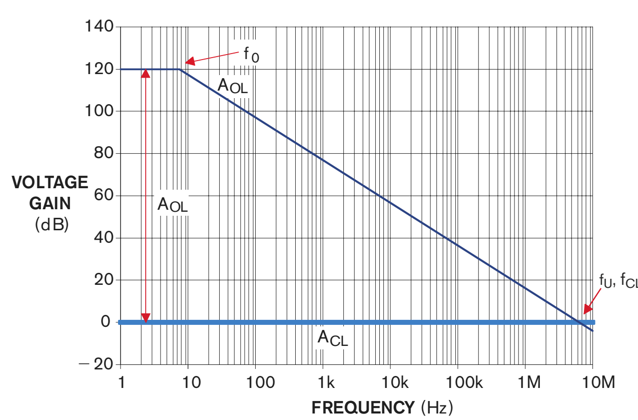

Figure 2 The open- and closed-loop-transfer function of the amplifier in **Figure 1** does not contain R_{IN} and C_{IN} as loads.

is greater than 20 dB/decade, the amplifier circuit will be marginally stable or completely unstable. For example, if the open-loop-gain curve, A_{OL}, is changing at −40 dB/decade, the amplifier circuit is unstable where the slope of the closed-loop-gain curve, A_{CL}, is zero at the intersection with the open-loop-gain curve.

You can evaluate the stability of the circuit in **Figure 1** with the op amp's open-loop-gain function, A_{OL} (**Figure 2**). The amplifier's dc open-loop gain is 120 dB. At approximately 7 Hz (f_0), the op amp's open-loop curve leaves 120 dB and progresses down at a rate of −20 dB/decade. As the frequency increases, this attenuation rate continues past 0 dB. The open-loop-gain curve, A_{OL}, crosses 0 dB at approximately 7 MHz (f_U). Because this curve represents a single-pole system, the crossover frequency, f_U, is equal to the amplifier's UGBW. This plot represents a stable system because the closure rate of the closed- and open-loop-gain curve is 20 dB/decade.

Figure 3 provides an accurate picture of the amplifier's performance minus the ADC's impact. Introducing the external RC on the op amp's output modifies the amplifier open-loop-gain curve.

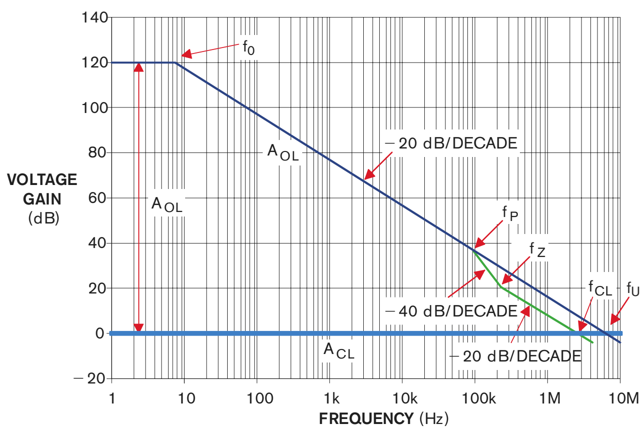

Figure 3 The pole, f_p, modifies the open-loop-gain curve of the amplifier by introducing a −20-dB/decade change to the −20-dB/decade slope of the open-loop-gain curve, making the slope −40 dB/decade. The added zero at frequency f_z changes the open-loop-gain curve back to −20 dB/decade.

When evaluating the amplifier's open-loop-gain curve with R_{IN} and C_{IN} in the circuit, you need to include the effect of the amplifier's open-loop output resistance, R_O. The combination of R_O, R_{IN}, and C_{IN} modifies the open-loop-response curve by introducing one pole, f_p (**Equation 1**), and one zero, f_z (**Equation 2**). The values of R_O, R_{IN}, and C_{IN} determine the corner frequency of f_p. The values of R_{IN} and C_{IN} determine the corner frequency of the zero.

$$f_P = \frac{1}{2\pi(R_0 + R_{IN})C_{IN}}. \qquad (1)$$

$$f_Z = \frac{1}{2\pi R_{IN} C_{IN}}. \qquad (2)$$

The pole, f_p, modifies the open-loop-gain curve of the amplifier by introducing a −20-dB/decade change to the already-−20-dB/decade slope of the open-loop-gain curve, making the slope equal to −40 dB/decade. The added zero at frequency f_z changes the open-loop-gain curve back to −20 dB/decade.

In the interest of stability, the effects of f_z must occur at a frequency lower than the intersect frequency of the open-loop- and closed-loop-gain curves (f_{CL}). **Figure 4** illustrates a condition in which f_z is higher than the open-loop/closed-loop-intersection frequency, f_{CL}. In this situation, the amplifi-

TABLE 1 SAR-ADC WORST-CASE SETTLING TIME

ADC Resolution (bits)	**K** (time-constant multiplier to ½-LSB accuracy)
8	6.24
10	7.62
12	9.01
14	10.4
16	11.78
18	13.17

Note: Using worst-case values, V_{IN}= full-scale voltage, or 2^N, and V_{SH0}=0V.

TABLE 2 MEASUREMENT RESULTS OF ADS7886 DIGITAL OUTPUT WITH OPA364

Time (nsec)		60	120	180	240	300	360	420	480	540	600	660	720
	Bin	**Frequency** (Hz)											
Histogram (code)	2044	0	0	0	0	0	0	0	0	0	0	0	0
	2045	0	0	0	0	0	0	0	0	0	0	0	0
	2046	4095	4095	4095	4095	4095	4095	4091	4052	4007	4001	3981	4028
	2047	0	0	0	0	0	0	4	43	88	94	114	67
	2048	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0
Sigma		0	0	0	0	0	0	0.031242	0.101946	0.145027	0.149778	0.164531	0.126877
Mean		2046	2046	2046	2046	2046	2046	2046.001	2046.011	2046.021	2046.023	2046.028	2046.016
Peak-to-peak noise (code)		0	0	0	0	0	0	0.2062	0.67284	0.957181	0.988533	1.085904	0.837385
		0	0	0	0	0	0	0.000977	0.010501	0.02149	0.022955	0.027839	0.016361

Note: Resistance is 66.5Ω, and input capacitance is 1500 pF for the relatively stable circuit.

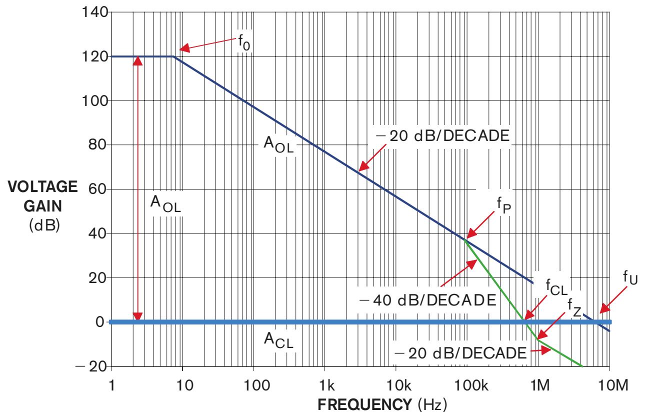

Figure 4 The pole and zero pair modify the amplifier's open-loop gain curve. R_{IN}, R_O, and C_{IN} generate the pole, causing a 40-dB/decade attenuation of the open-loop-gain plot. R_{IN} and C_{IN} generate the zero, which occurs after the frequency of the modified open-loop/closed-loop intersection (f_{CL}).

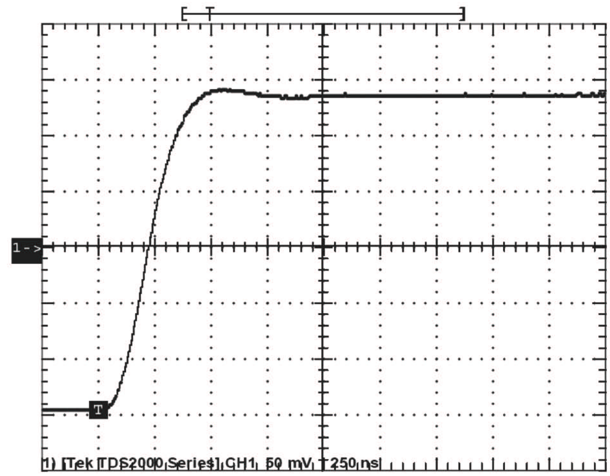

Figure 5 Measuring a 280-mV-p-p, small-signal step response (250 nsec/division, 50 mV/division) at V_{IN} with the OPA364 op amp yields an input resistance of 66.5Ω and an input capacitance of 1500 pF.

er circuit is marginally stable, with a phase margin of less than 45°. For this circuit, marginal stability can occur if the closure rate between the open- and closed-loop-gain curves is greater than 20 dB/decade.

You can find the modified closed-loop bandwidth, f_{CL}, by using the amplifier UGBW, the open-loop gain at the pole frequency (f_P), and the modified open-loop gain at the zero frequency (f_Z). The following **equations** describe the curves in **figures 2** and 3 and identify f_{CL}:

$$G_P = -20\log\left(\frac{f_P}{f_U}\right), \quad (3)$$

$$G_Z = G_P - 40\log\left(\frac{f_Z}{f_P}\right), \quad (4)$$

$$G_{CL} = G_Z - 20\log\left(\frac{f_{CL}}{f_Z}\right), \text{ if } G_Z > 0 \text{ dB}, \quad (5)$$

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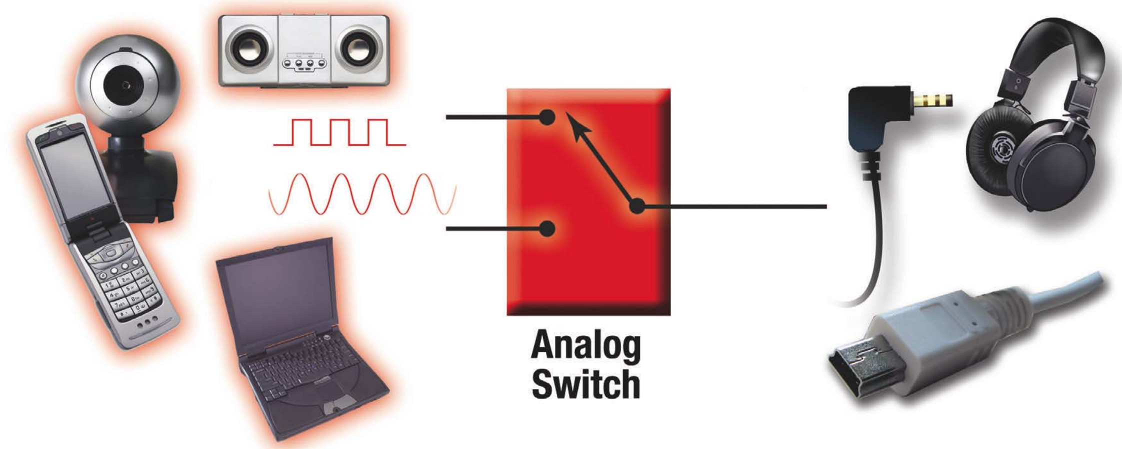

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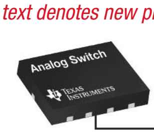
TS5A23166	SPST x 2	0.9	0.25	0.1	1.65	5.5	2 kV HBM	7.5	11	US8-8, WCSP-8
TS3A4751	SPST x 4	0.9	0.4	0.05	1.65	3.6	4 kV HBM	14	9	TSSOP-14, **SON-14, µQFN-14**
TS5A6542	SPDT	0.75	0.25	0.25	2.25	5.5	15 kV Contact (IEC L-4)	25	20	WCSP-8, µQFN-8
TS5A3159A	SPDT	0.9	0.25	0.1	1.65	5.5	2 kV HBM	30	20	SC70-6, SOT23-6, WCSP-6
TS5A12301E	SPDT	0.75	0.1	0.1	2.25	5.5	8 kV Contact (IEC L-4)	225	215	WCSP-6
TS5A23159	SPDT x 2	0.9	0.25	0.1	1.65	5.5	2 kV HBM	13	8	MSOP-10, QFN-10
TS3A24159	SPDT x 2	0.3	0.04	0.05	1.65	3.6	2 kV HBM	35	25	WCSP-10, SON-10, VSSOP-10
TS5A26542	SPDT x 2	0.75	0.25	0.25	2.25	5.5	15 kV Contact (IEC L-4)	25	20	WCSP-12
TS5A22362/4	SPDT x 2	0.94	0.46	0.11	2.3	5.5	2.5 kV HBM	80	70	WCSP-12, SON-10, VSSOP-10
TS3USB221	SPDT x 2	6	1	0.2	2.3	3.6	2 kV HBM	30	12	SON-10, µQFN-10
TS3A44159	SPDT x 4	0.45	0.1	0.07	1.65	4.3	2 kV HBM	23	32	TSSOP-16, SON-16, µQFN-16
TS5A3359	SP3T	0.9	0.25	0.1	1.65	5.5	2 kV HBM	21	10.5	US8-8, WCSP-8
TS3A5017	SP4T x 2	12	9	2	2.3	3.6	2 kV HBM	9.5	3.5	TVSOP-16, SON-16, **µQFN-16**

Red text denotes new products and new package addition



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TEXAS INSTRUMENTS

TABLE 3 MEASUREMENT RESULTS OF ADS7886 DIGITAL OUTPUT WITH OPA364

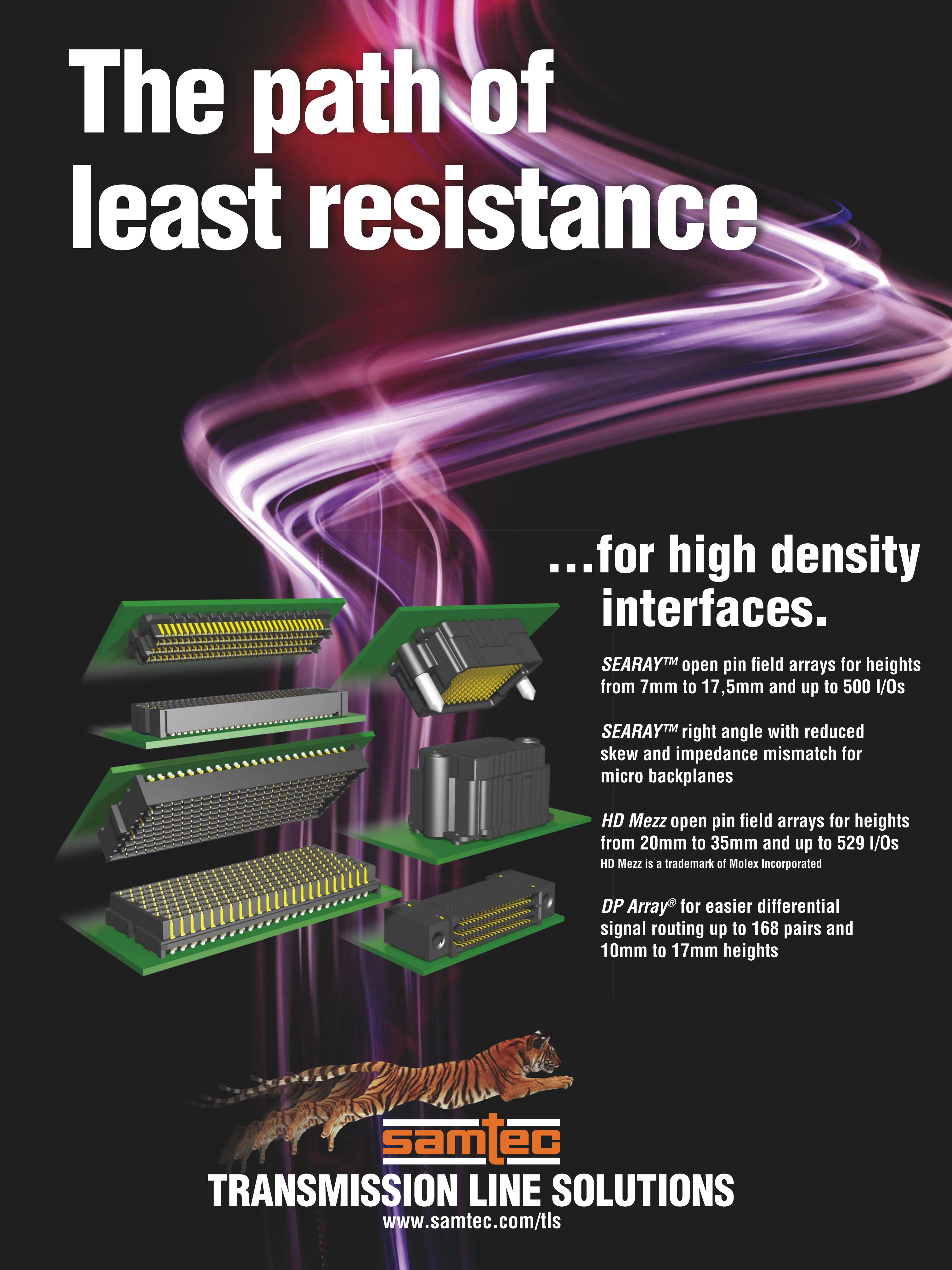
Time (nsec)		60	120	180	240	300	360	420	480	540	600	660	720
	Bin	**Frequency** (Hz)											
	2044	0	0	0	0	0	0	0	0	0	0	0	0
	2045	0	0	0	0	0	0	0	0	0	0	0	0
	2046	3617	4070	4091	4095	4095	4084	3707	1708	1370	1654	2230	3278
Histo-gram (code)	2047	465	25	4	0	0	11	387	2284	2528	2355	1833	817
	2048	13	0	0	0	0	0	1	103	197	86	32	0
		0	0	0	0	0	0	0	0	0	0	0	0
Sigma		0.334518	0.077905	0.031242	0	0	0.051765	0.294074	0.537307	0.548346	0.527598	0.514143	0.399682
Mean		2046.12	2046.006	2046.001	2046	2046	2046.003	2046.095	2046.608	2046.714	2046.617	2046.463	2046.2
Peak-to-peak noise (code)		2.207819	0.514174	0.2062	0	0	0.341651	1.940889	3.546228	3.619084	3.482145	3.393341	2.637901
		0.119902	0.006105	0.000977	0	0	0.002686	0.094994	0.608059	0.713553	0.617094	0.463248	0.199512

and

$$f_{CL} = (f_Z)\left(10^{(G_Z/20)}\right), \quad (6)$$

where G_P is the gain in decibels of the open-loop-gain curve at f_P, G_Z is the gain in decibels of the modified open-loop-gain curve at f_Z, and G_{CL} is the gain in decibels of the closed-loop-response frequency where the closed-loop response intersects with the modified open-loop-gain curve.

The frequency distance between the pole and zero must be equal to or less than one decade. This requirement is necessary because the phase change from zero negates the phase changes that the pole initiates. Note that the pole formula (**Equation 1**) includes R_{IN} and R_O; the formula for zero (**Equation 2**) includes only R_{IN}. If the distance between the pole and zero exceeds one decade, the phase response will not "recover" in time, and the output of the circuit will show more ringing.



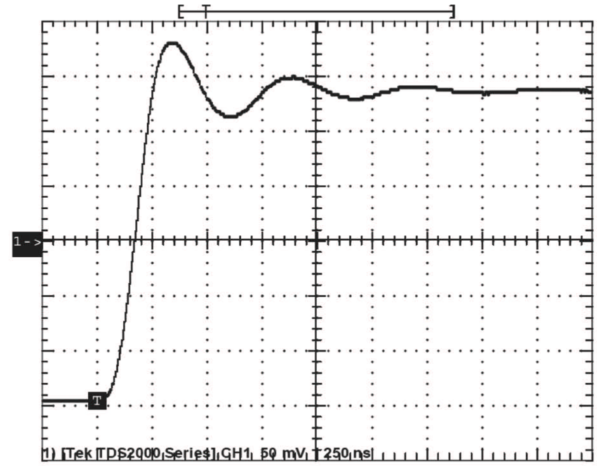


Figure 6 Measuring a 280-mV-p-p, small-signal step response (250-nsec/division, 50-mV/division scales) at V_{IN} with the OPA364 op amp yields an input resistance of 15Ω and an input capacitance of 1500 pF.

$$R_{IN} \geq \frac{R_O}{9}. \quad (7)$$

CORRECT VALUES OF R_{IN} AND C_{IN}

The primary purpose of capacitor C_{IN} is to charge the ADC's input sampling capacitor, C_{SH}, during the ADC's signal acquisition. With C_{IN} in the circuit, the amplifier should provide less than 5% of the charge to C_{SH} during signal acquisition, and C_{IN} provides more than 95% of the required charge. To ensure that C_{IN} provides most of the charge to the ADC's input during acquisition, C_{IN} should be greater than or equal to 20 times C_{SH} (**references 2** and **3**).

R_{IN} serves as the isolation resistor between the op amp and C_{IN}. R_{IN} assists in stabilizing the amplifier, but its secondary task is to ensure that the system can charge the input ADC capacitor in a timely fashion (**Reference 3**). The time-constant multiplier of this ADC acquisition time is K. As a first step, with these two variables and C_{IN},

$$R_{IN} \approx \frac{t_{ACQ}}{K \times C_{IN}}, \quad (8)$$

where t_{ACQ} is the ADC's acquisition time (**Reference 4**).

AMPLIFIER-FREQUENCY AND GAIN VALUES

As a first step to optimization, look at the C_{IN} and op-amp characteristics. During op-amp production, internal components can vary. Capacitances can change by as much as ±15%. Additionally, the op-amp transistor's transconductance can vary from ±5 to ±15%. So, if you are looking for a variation of f_U at 25°C with three times sigma, you can use ±20% as a good starting point.

It is good practice to use $f_{CL}=f_U/2$ and $f_Z=f_{CL}/2$ or $f_Z=f_U/4$ for good stability over different production lots. If these conditions are a concern, having G_Z equal to 6 dB or $f_Z=f_{CL}/2$ further stabilizes the system from production lot to production lot.

Using these gain and frequency points' definitions, you can make decisions about the best values for R_{IN} and C_{IN}. If you define G_Z as equal to 3 dB, then 0 dB=3 dB−20×log(f_{CL}/f_Z)

(**Equation 5**) or $f_{CL}=1.41\times f_Z(f_Z=f_{CL}/1.41)$. If you want $G_Z=6$ dB, then $0\text{ dB}=6\text{ dB}-20\times\log(f_{CL}/f_Z)$, or $f_{CL}=2\times f_Z(f_Z=f_{CL}/2)$.

PROOF OF CONCEPT

This theory is a good start, but proof of concept completes the picture. Two sample circuits tie this theory to reality. These designs use the OPA364 as the op amp with a UGBW of 6.45 MHz and open-loop output resistance, R_O, of 110Ω. Both designs also use a 1500-pF capacitor for C_{IN}. The target closed-loop bandwidth, f_{CL}, in the design is $f_U/2$, or 3.23 MHz, and the target frequency of added zero is $f_U/4$, or 1.61 MHz.

Two conditions are observable using an R_{IN} of 66.5Ω (Design 1, the relatively stable circuit) and 15Ω (Design 2, the marginally stable circuit). You can then observe the effects of a small-signal step response at the test point, V_{IN}. The op amps are in a buffer configuration, with a 1V/V closed-loop gain. The second series of tests uses the ADS7886 for the SAR ADC.

In the first design, R_{IN} is 66.5Ω. Combining the effects of C_{IN}, R_{IN}, and R_O produces a pole frequency, f_P (**Equation 1**), at 601 kHz with an open-loop gain, G_P (**Equation 3**), of 20.6 dB. This combination of C_{IN}, R_{IN}, and R_O also produces a zero, f_Z (**Equation 2**), at 1.596 MHz with an open-loop gain, G_Z (**Equation 4**), of 3.65 dB. **Figure 3** shows the system's Bode plot. **Figure 5** shows the response of V_{IN} when the noninverting input of the op-amp buffer sees a 280-mV-p-p, small-signal step response. The signal at V_{IN} is stable within 1 μsec. This condition is desirable for this SAR ADC.

In the second design, R_{IN} is 15Ω. With the values of R_{IN}, C_{IN}, and R_O, the pole frequency, f_P, is 849 kHz at an open-loop gain, G_P, of 17.6 dB. The zero frequency, f_Z, is 7.074 MHz with an open-loop gain, G_Z, of −19.22 dB. **Figure 4** shows the system's Bode plot. **Figure 6** shows the response of V_{IN} when the noninverting input of the op-amp buffer sees a 280-mV-p-p, small-signal step response.

This marginally stable test circuit generates an overshoot with ringing, which is undesirable. The ADS7886 produces an unstable and inaccurate result from the signal in **Figure 6**.

These measurements show how the system responds to an input step without the ADS7886 connected. You can expect similar results when the load changes with the ADS7886. Closing the ADS7886 sampling switch generates a kickback current. Adding the ADS7886 to the circuit makes it difficult to observe 12-bit-accurate changes with an oscilloscope. Therefore, you apply a new measurement technique.

The test begins with the addition of the ADS7886 to the circuit (**Figure 1**). This circuit applies a constant voltage at the noninverting input of the OPA364. Testing began with an ADS7886 acquisition time of 300 nsec and 4096 measurements; testing continued with an acquisition time of 60 nsec, again with 4096 measurements. The acquisition time continued to increase by increments of 60 nsec until the test was complete for both designs.

After collecting this data, calculations of sigma and mean values for every ADS7886 acquisition point yield the results in **tables 2** and **3**. In the **tables**, the top line identifies the additional acquisition for the ADS7886 beyond the initial acquisition time of 300 nsec from test to test. The far left column lists the output-data codes and the number of times these codes appear in the body of the **table**. The statistical summary of the body of both **tables** appears at the bottom.

The data shows that the stable design has a lower sigma and more consistent mean. The mean value of the unstable system has an error of more than 0.7 LSB, whereas the stable system has an error of less than 0.03 LSB.

DESIGNING THE ADC SYSTEM

Choosing the right op amp for the ADC is critical. Be sure to compare issues such as amplifier noise, bandwidth, and settling time to the ADC's SNR, SFDR (spurious-free dynamic range), input impedance, and sampling time. The primary purposes of capacitor C_{IN} are to provide charge to the ADC's input sampling capacitor, C_{SH}, during the ADC's signal-acquisition time and to offload the amplifier from dynamic activity from the ADC. The proper design equation when determining C_{IN} is:

$$20\times C_{SH} \le C_{IN} \le 60\times C_{SH}. \quad (9)$$

Determining this value allows you to calculate the new time-constant multiplier, K_1, with N equal to the number of ADC bits:

$$K_1 = \ln\left[\frac{2^{N+1}}{(C_{IN}/C_{SH}+1)}\right]. \quad (10)$$

As design requirements and ADC performances set up the ADC's acquisition times, calculate the frequency of the added zero, f_Z:

$$f_Z = \frac{K_1}{2\pi t_{ACQ}}. \quad (11)$$

After determining these quantities, verify that the system is stable with this **equation**:

$$f_Z \le ¼ f_U. \quad (12)$$

With the frequency of the added zero and C_{IN}, determine the value of R_{IN} using the following two **equations**:

$$R_{IN} = \frac{1}{2\pi\times C_{IN}\times f_Z}. \quad (13)$$

$$R_{IN} \ge \frac{R_O}{9}. \quad (14)$$

Calculate the frequency of the added pole, f_P:

$$f_P = \frac{1}{2\pi\times(R_{IN}+R_O)\times C_{IN}}. \quad (15)$$

Check the gain of the added zero on the modified open-loop-gain curve. For a stable design, this value needs to be greater than or equal to 6 dB:

$$6\text{ dB} \le G_Z = -20\log\left(\frac{f_P}{f_U}\right) - 40\log\left(\frac{f_Z}{f_P}\right). \quad (16)$$

Once the design process is complete, it is critical that you benchtest the circuit to verify stability. **EDN**

ACKNOWLEDGMENT

Special thanks to Tim Green for his help in developing this article.

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AUTHORS' BIOGRAPHIES

Miro Oljaca is a senior applications engineer at Texas Instruments, where he is responsible for high-precision linear products focusing on industrial applications. Oljaca has more than 20 years of design experience in motor control and power conversion. He received bachelor's and master's degrees in electrical engineering from the University of Belgrade (Serbia) and is a member of AEI, CNI, IEE, and IEEE.

Bonnie Baker is a senior applications engineer at Texas Instruments and has been involved with analog and digital designs and systems for nearly 20 years. Baker has written more than 250 articles, design notes, and application notes. She is the author of A Baker's Dozen: Real Analog Solutions for Digital Designers *and the co-author of* Circuit Design: Know It All *and* Analog Circuits: World-Class Designs. *In addition, Baker writes the column "Baker's Best" for* EDN.

Precision analog bests digital in speed, noise, simplicity, and ease of implementation

Paul Antonucci, Alberti's Window, Watertown, MA

Every once in a while, I read that analog is on the way out, and everything should be digital. Recently, I was involved in a design project that illustrates that this belief doesn't apply in many situations.

The problem was to put two new optical breaks into the drive mechanism of a group of robotically controlled, Internet-accessible telescopes in an education application. The drive mechanisms have been showing signs of wear from excess slipping at end of travel: The sensors would signal end of travel, so there would be no slipping. The fork arms and other locations enclosed the internal wiring harnesses of the telescopes so that rewiring the telescopes would have been awkward.

So, the best idea was to encode the signals from the new sensors into the current wiring. There was one digital signal available; the challenge was to encode the two new sensors onto that signal.

Using a digital approach would have involved adding a small microcontroller to the base and encoding a serial digital signal to send up the tube, with appropriate synchronous pulses, data, and check sums, which then would undergo decoding at the CPU. This approach would have required some sort of reset provision because the telescope needed to operate independently for months, and those serial digital signals would have undesirable switching noise on them. The CPU would also have had to spend time grabbing, decoding, and synchronizing the signals, taking up more time. In addition, we would have had to have written some messy bit-banging code: not a huge challenge—but not a simple or elegant one, either.

Instead, this approach uses a variation on a simple adder circuit in which each sensor contributes a different amount. Taking the basic binary idea that one sensor adds ±1; the next, ±2; and the last, ±4, the approach uniquely represents each state.

The basic requirements are a voltage reference, some op amps, and a summing junction. This application uses IC_4, a Texas Instruments (www.ti.com) REF3040 voltage reference, which has an output tolerance of 0.2% yet costs only approximately $1 (**Figure 1**). This reference generates a voltage of 4.096V and produces enough current to run the op amps, which run rail to rail to within a few millivolts. Be careful, however: Some "rail-to-rail" op amps have insufficient current drive near the rails. This circuit uses 0.1%-precision resistors, which cost only about 20 cents. Remember that you can use two 10-kΩ resistors in series and two in parallel to create the 20- and 5-kΩ resistances that you see in the **figure**. The assembly and bill of materials are simpler and precision is better because the distributions around the ideal resistor value tend to cancel out. **Table 1** lists the predicted output voltages.

TABLE 1 PREDICTED OUTPUT VOLTAGES

Sensor 1	Sensor 2	Sensor 3	Output
0	0	0	0.256
0	0	1	0.768
0	1	0	1.28
0	1	1	1.792
1	0	0	2.304
1	0	1	2.816
1	1	0	3.328
1	1	1	3.84

Tests with a voltmeter show that all output voltages were within 1 mV of the predicted output values. The error budget of less than 1% shows that you could use this method to encode several more sensors. In the telescope, the CPU's ADC reads the outputs. Read it twice to ensure that you aren't catching it at a transi-

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tion. The advantages of the circuit include the fact that its dc signals ensure that there's no noise and that the updates are nearly instantaneous. Also, because op amps are simple, virtually indestructible, and insensitive to noise, no reset circuits are necessary. Best of all, the design requires no programming.EDN

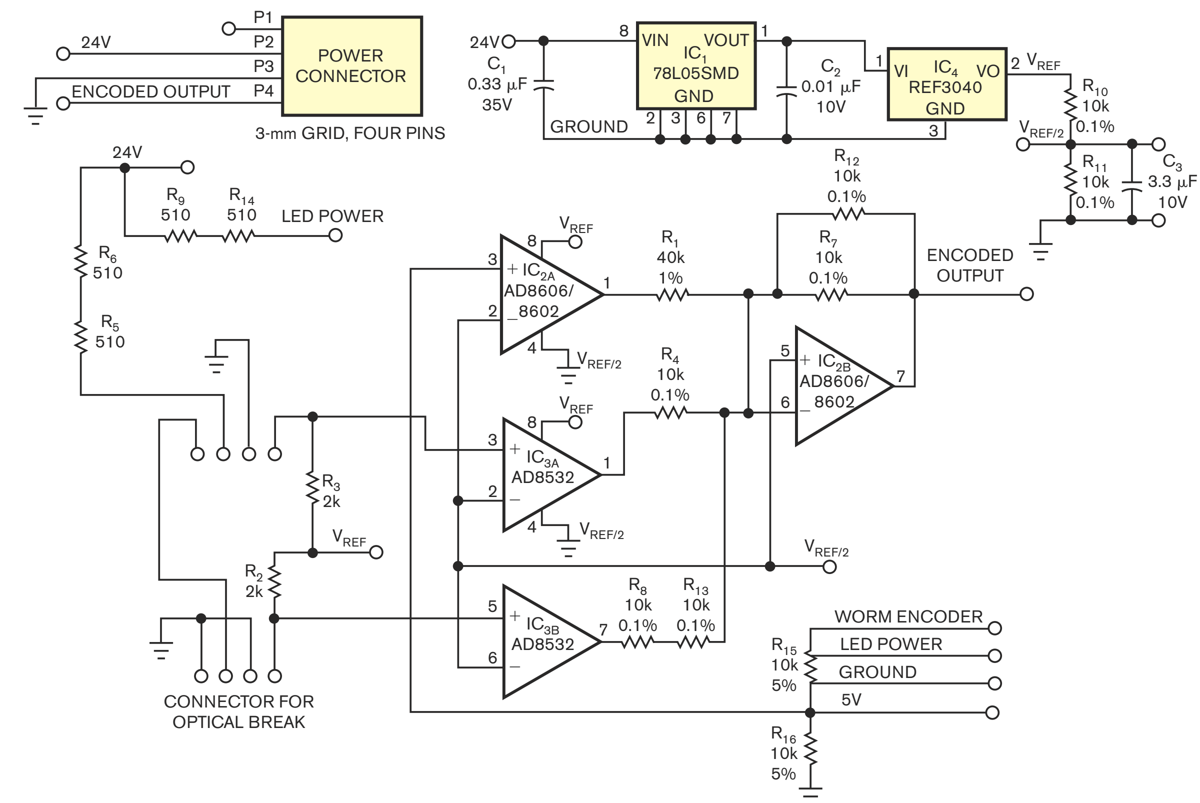

Figure 1 This application uses IC_4, a REF3040 voltage reference, which has an output tolerance of 0.2% yet costs only approximately $1.

Mutliplexing technique yields a reduced-pin-count LED display

Saurabh Gupta and Dhananjay V Gadre,
Netaji Subhas Institute of Technology, Dwarka, New Delhi, India

"Charlieplexing" as a method of multiplexing LED displays has recently attracted a lot of attention because it allows you, with N I/O lines, to control N×(N−1) LEDs (**references 1** through **5**). On the other hand, the standard multiplexing technique manages to control far fewer LEDs. **Table 1** lists the number of LEDs that you can control using Charlieplexing and standard multiplexing by splitting the available number of N I/O lines into a suitable number of rows and columns. **Table 1** also shows the duty cycle of the current that flows through the LEDs when they are on.

Clearly, Charlieplexing allows you to control a much larger number of LEDs with a given number of I/O lines. However, the downside of this technique is the reduced duty cycle of the current that flows through the LEDs; thus, to maintain a given brightness, the peak current through the LEDs must increase proportionately. This current can quickly reach the peak-current limit of the LED. Nonetheless, Charlieplexing is a feasible technique for as many as 10 I/O lines, allowing you to control as many as 90 LEDs. To control an equivalent number of LEDs using the standard

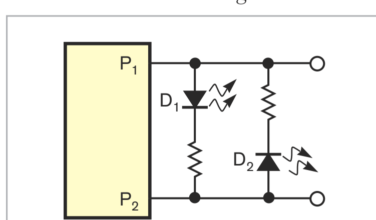

Figure 1 "Charlieplexing" with two I/O lines allows you to control two LEDs.

TABLE 1 NO. OF LEDs AND DUTY CYCLE

No. of I/O lines	Multiplexing-controlled LEDs	Duty cycle with multiplexing (%)	Charlieplexing-controlled LEDs	Duty cycle with Charlieplexing (%)
Two	Two	100	Two	50
Three	Three	100	Six	16.67
Four	Four	50	12	8.33
Five	Six	50	20	5
Six	Nine	33	30	3.33
Seven	12	33	42	2.4
Eight	16	25	56	1.78
Nine	20	25	72	1.38
10	25	20	90	1.11

TABLE 2 OUTPUT VOLTAGE

P_1	P_2	Voltage at node PR_1
0	0	V_{CC}
0	1	V_{CC}
0	Z	V_{CC}
1	0	0
1	1	0
1	Z	0
Z	0	$V_{CC}/2$
Z	1	$V_{CC}/2$
Z	Z	$V_{CC}/2$

TABLE 3 I/O LINES AND PR_1 VOLTAGE

P_1	P_2	Voltage at node PR_1	LED that turns on
0	0	V_{CC}	L_3
0	1	V_{CC}	L_2
1	0	0	L_1
1	1	0	L_4
Z	Z	$V_{CC}/2$	None

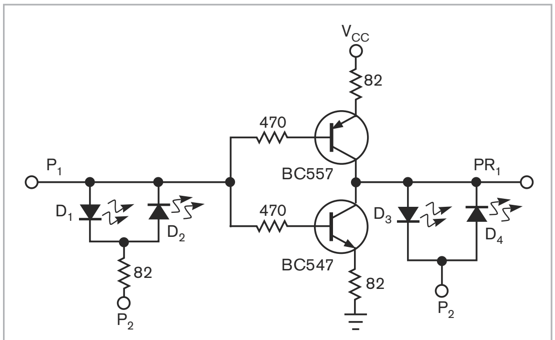

Figure 2 "GuGaplexing" with two I/O lines allows you to control four LEDs.

multiplexing technique would require 19 I/O lines.

This Design Idea proposes a modification to the Charlieplexing technique that allows you to control twice as many LEDs. Thus, the proposed method, "GuGaplexing," allows $2 \times N \times (N-1)$ LEDs using only N I/O lines and a few additional discrete components (**Figure 1**). To turn on LED D_1 using the Charlieplexing method, set P_1 to logic one and P_2 to logic zero. To turn on LED D_2, set P_1 to logic zero and P_2 to logic one. **Figure 2** shows the proposed GuGaplexing scheme with two I/O lines controlling four LEDs. The GuGaplexing technique exploits the fact that each I/O line has three states: one, zero, and high impedance. Thus, with two I/O lines, states 00, 01, 10, and 11 of eight possible states control the LEDs.

Table 2 lists the voltage at the output of the transistor pair for various states of the two I/O lines, P_1 and P_2. The transistor pair comprises a BC547 NPN and a BC557 PNP transistor; matched transistor pairs are recommended. For N I/O lines, the GuGaplexing technique requires $N-1$ transistor pairs. **Table 3** shows the state of the I/O lines P_1 and P_2 and the voltage at node PR_1 to control the four LEDs. The circuit requires that the LED turn-on voltage should be slightly more than $V_{CC}/2$. Thus, for red LEDs with a turn-on voltage of approximately 1.8V, a suitable supply voltage is 2.4V. Similarly, for blue or white LEDs, you can use a 5V supply voltage. Modern microcontrollers, especially the AVR series of microcontrollers from Atmel (www.atmel.com), operate at a wide variety of supply voltages ranging from 1.8 to

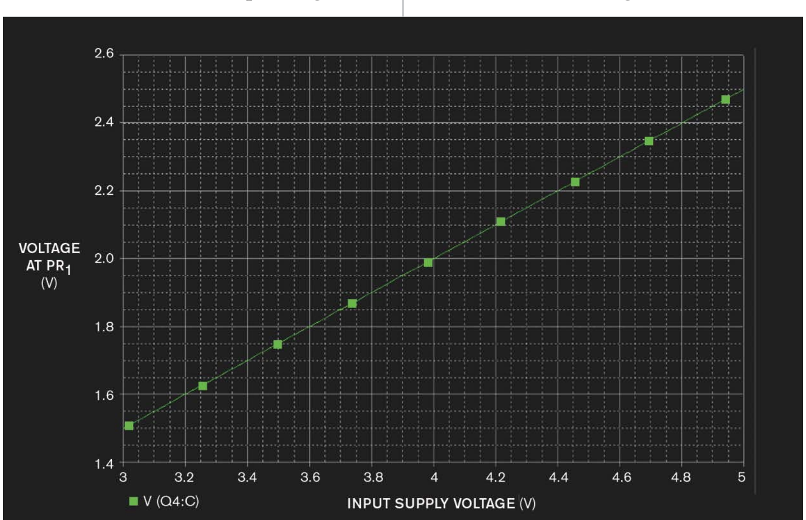

Figure 3 This graph plots the voltage at node PR_1 for various supply-voltage values when the input to the transistor pair is floating.

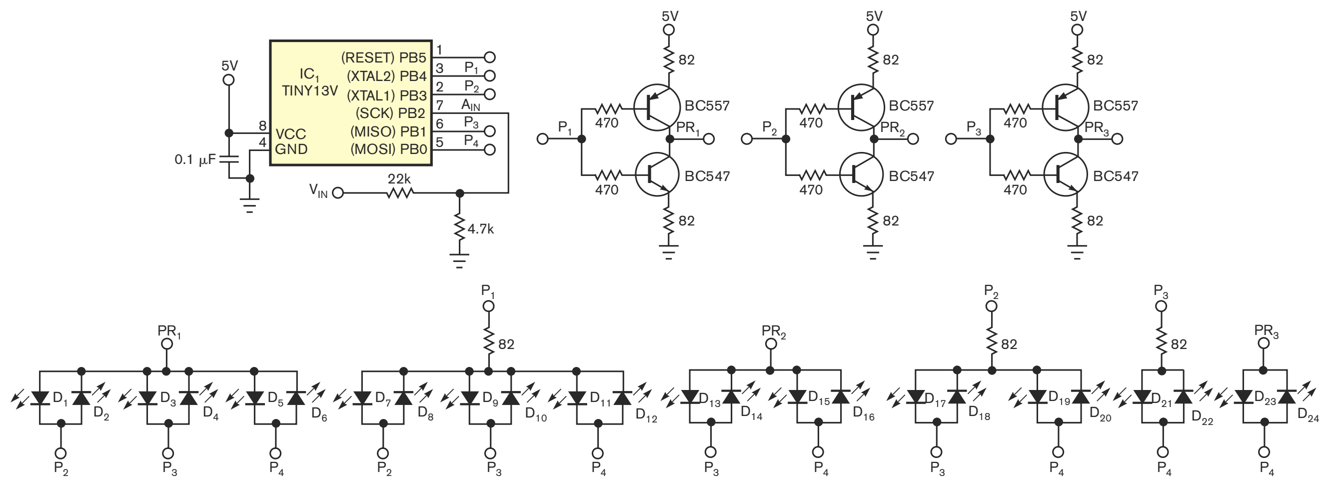

Figure 4 With the GuGaplexing technique, controlling 24 LEDs requires only four I/O lines and three sets of transistors.

5.5V, and this design uses a Tiny13 microcontroller to implement the GuGaplexing technique.

Figure 3 plots the voltage at node PR_1 for various supply-voltage values when the input to the transistor pair is floating. The Spice simulation ensures that the circuit would work properly to provide $V_{CC}/2$ at the PR_1 node for wide operating-supply-voltage values when the input is floating.

A 24-LED bar display validates the scheme in a real application (**Figure 4**). The display is programmable and uses a linear-display scheme for the input analog voltage. The input analog voltage displays in discrete steps on the 24-LED display. Controlling 24 LEDs requires only four I/O lines and three pairs of transistors. The system uses 5-mm, white LEDs in transparent packaging and a 5V supply voltage. The GuGaplexing implementation uses an AVR ATTiny13 microcontroller. The analog input voltage connects to Pin 7 of the ADC input of the Tiny13 microcontroller.

The control program for the ATTiny13 microcontroller is available with the Web version of this Design Idea at www.edn.com/081016di1. The source code is in C and was compiled using the AVRGCC freeware compiler. You can modify the source code to display only one range of input voltage between 0 and 5V. For example, it is possible to have a linear-display range of 1 to 3V or a logarithmic scale for input voltage of 2 to 3V. EDN

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Derive a simple high-current source from a lab supply

Roger Griswold and Alfredo Saab,
Maxim Integrated Products, Sunnyvale, CA

When electronic testing requires an adjustable current source, you must often build that piece of test equipment in the lab. You can easily make such a current source from a standard force-sense lab power supply (**Figure 1**). The circuit requires an additional power supply for the ICs and a separate control voltage. The feedback signal to the force-sense supply comes from a MAX4172 high-side current monitor from Maxim (www.maxim-ic.com). In the configuration in **Figure 1**, the circuit offers a 1-to-1 ratio of control voltage to load current (1A/V). **Figure 2** shows load current as a function of load resistance.

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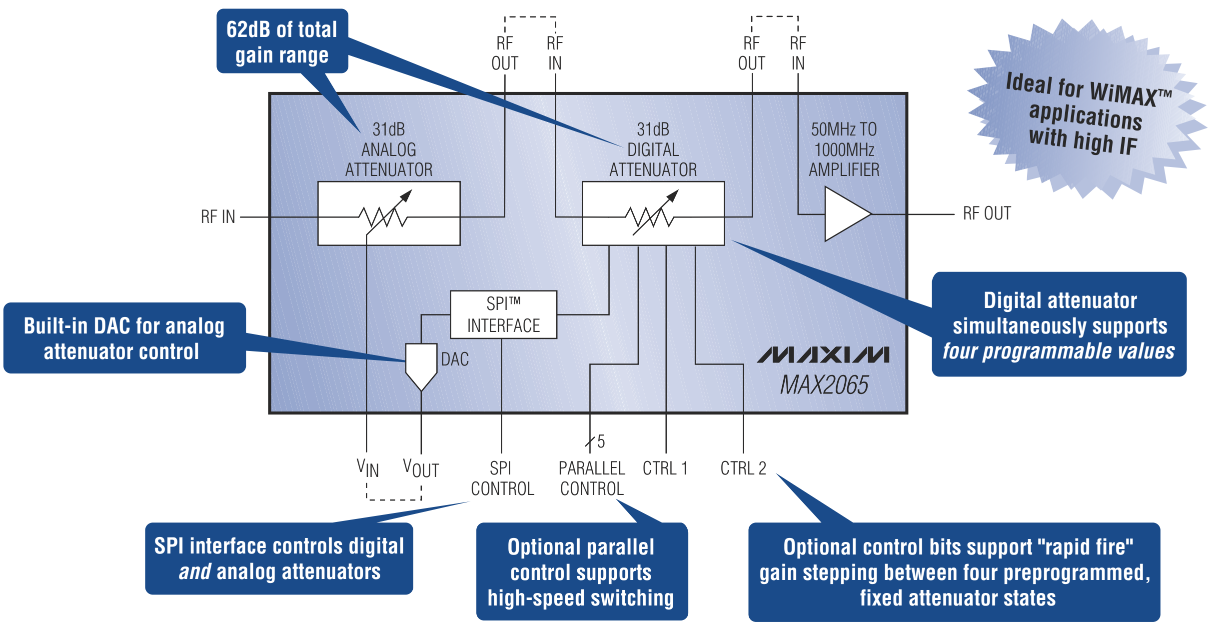

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Part	VGA Type	Frequency (MHz)	Gain Range (dB)	Digital Gain Steps (dB)	OIP3 (dBm)	OIP2 (dBm)	OP_{1dB} (dBm)	HD2 (dBc)	HD3 (dBc)	NF (dB)
MAX2065	Analog/digital	50 to 1000	-43 to +19	1	41.5	60	18.5	-63	-80	6.6
MAX2066	Digital	50 to 1000	-11 to +20	1	42	60.5	18.5	-63	-80	5.5
MAX2067	Analog	50 to 1000	-9.5 to +21.5	—	42	61	18.5	-63	-80	4.2

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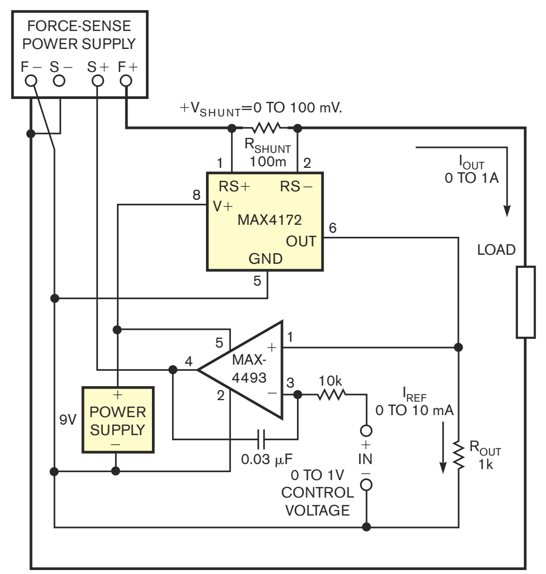

Figure 1 Adding these components to a standard force-sense lab supply makes a simple voltage-controlled current source. As configured, the circuit produces a control ratio of 1-to-1A/V.

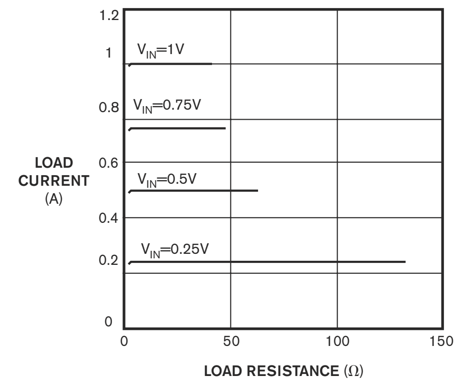

Figure 2 This graph shows load current versus load resistance for the circuit in **Figure 1**.

maximum allowed voltage of 150 mV between the RS+ and RS− terminals, the maximum positive RS voltage of 32V, and the maximum current capability of the force-sense supply all limit the output current of the supply.

Because voltage and current meters in the force-sense supply display inaccurate values while this circuit is operating, you should use external meters to monitor the load voltage and load current. Also, be aware that, if you remove the load so that the output current is 0A, the open-circuit voltage of the force-sense supply goes to the maximum value it can generate.**EDN**

DESIGN NOTES

Power Monitor for Automotive and Telecom Applications Includes ADC and I²C Interface – Design Note 452

Dilian Reyes

Introduction

The LTC®4151 is a high side power monitor that includes a 12-bit ADC for measuring current and voltage, as well as the voltage on an auxiliary input. Data is read through the widely used I²C interface. An unusual feature in this device is its 7V to 80V operating range, allowing it to cover applications from 12V automotive to 48V telecom.

Automotive Power Monitoring

Automobile batteries serve more systems than ever before, many of which operate when the battery is not charging, such as information/entertainment systems or devices plugged into the accessory socket.

The high input voltage of the LTC4151 is a good fit for monitoring power in high transient environments such as automotive. Figure 1 shows the LTC4151 monitoring up to 16A through a 5mΩ sense resistor at an accessory socket, and feeding data via I²C to a microcontroller.

A portable GPS unit is used to illustrate the principle. In this case it is powered up and charging its own internal battery, drawing 396mA from the 12.1V supply. The 4.8W of power is relatively low and thus calls for no immediate need for alarm. However, a higher power device such as a built-in DVD player with dual LCD displays or an external 60W thermoelectric cooler plugged into the accessory socket would drain the battery considerably faster than the GPS. The digital information from the LTC4151 high resolution and accurate 12-bit ADC can be interpreted and displayed on an in-dash screen, or used by the host system to shut down the channel to avoid fully draining the battery.

Telecom Power Monitoring with PoE

One major advantage of the wide range input voltage of the LTC4151 is the ability to monitor higher voltage applications such as those used in telecommunications. The emerging IEEE802.3af Power over Ethernet (PoE) standard has gained much interest in the past few years.

In Figure 2 the LTC4151-1 monitors the isolated 48V power supply to the LTC4263 single port Power Sourcing Equipment (PSE) controller. Communication across isolation through optocouplers to a microcontroller is simplified with the LTC4151-1's split bidirectional SDA line to separate data in and data out. Pull-up resistors tie directly to the 48V supply for pins SCL and SDAI, which are internally clamped to 6V, and inverted SDAO is configured to be clamped by an optocoupler diode. With the low speed optocouplers shown, the LTC4263 generating its own

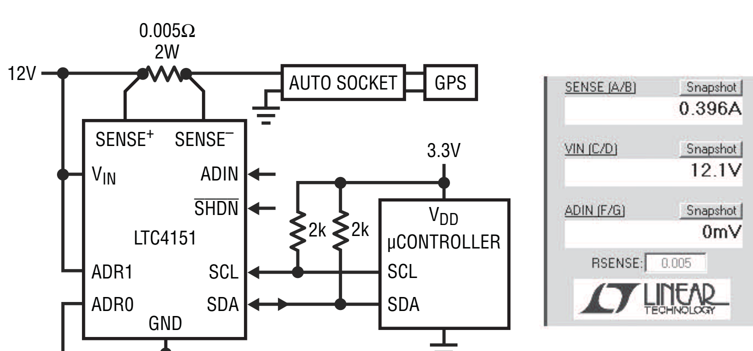

Figure 1. The LTC4151 Monitoring Voltage and Current of an Auto Socket with a GPS Unit

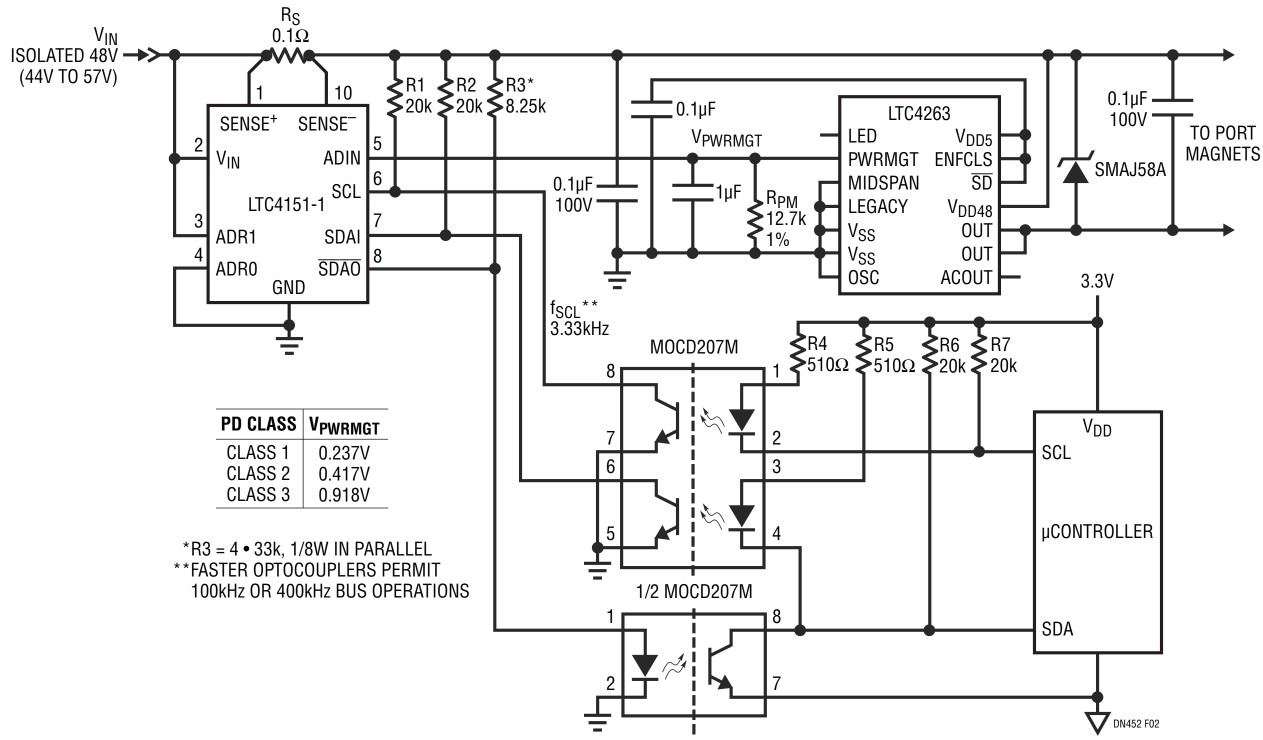

Figure 2. The LTC4151-1 in a PoE Single Port PSE with the LTC4263. I²C Communication to an Isolated Microcontroller

5V supply, and the LTC4151 high voltage protected I²C pins, a separate digital supply is not needed on the PoE side, just the single isolated 48V supply.

Optional power classes (4W, 7W and 15.4W) categorize the power requirements of a Powered Device (PD) on the cable end. The LTC4263 outputs a current to a power management resistor that is proportional to the power class of the plugged-in PD. The LTC4151-1 measures the resulting voltage through its auxiliary ADC input and reports this to the microcontroller, which in turn interprets what power class is present. The microcontroller can then read the current being drawn at the port to determine if the PD is abiding by its power class, and confirm that the supply voltage to the PSE controller meets PoE standards.

The LTC4151 has a configurable address so multiple LTC4151s can operate on the same bus, allowing for a multiport solution with monitoring at each port. This assists with the controller power management functions, which utilizes the available power from an optimized supply to the individual ports.

Additional benefits of the LTC4151 is the integrated current sense amplifier, input voltage resistor divider, precise ADC reference voltage and channel select MUX. These improve accuracy versus variances of external components and also save on costs of discrete parts.

Conclusion

The LTC4151 is an easy to use but feature-rich power monitoring device suitable for a wide variety of automotive, telecom and industrial applications. It provides accurate voltage and current monitoring of a positive supply rail from 7V to 80V via a simple I²C interface.

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LINKING DESIGN AND RESOURCES

Programming presents opportunity for distribution

With forecasters projecting that the programmable-IC market will grow at a CAGR (compound-annual-growth rate) of more than 17% from 2007 to 2011, components distributors are taking notice. "From a distributor's perspective, if you look at the amount of semiconductor products that all of us, Avnet and its competitors, sell, … you could argue that at least a third or more of the sales are probably in programmable products of one kind or another," says Jim Smith (**photo**), president of Avnet Logistics. "Obviously, those programmable products need to be programmed."

Hence, Avnet Inc (www.avnet.com) recently acquired Source Electronics Corp, a 20-year-old provider of outsourced custom-programming services. Avnet has incorporated the Hollis, NH-based company into its Avnet Logistics business. With facilities around the globe, Source supports customers in a variety of end markets, including consumer electronics, automotive, mobile communications, telecommunications, networking, computing, and enterprise storage, through programming services that use proprietary programming processes and result in low defect rates and rapid order fulfillment.

"If you look at [Avnet Electronics Marketing] globally, design is the core of our business. We hire FAEs [field-application engineers], and we go to market from a technical perspective. That group designs in programmable ICs; then there has to be someone to help our customers program those ICs. Source is invested in technology that helps develop algorithms and assists the various companies where there is a technical application associated with the programming of the IC," Smith says. "We see a huge opportunity."

At the estimated CAGR, programmable ICs will be a $50 billion market in 2011. "That's a nice market to play in," he says.

GREEN UPDATE

EU RECHARGES BATTERY DIRECTIVE

The EU (European Union) has implemented its New Batteries Directive, prohibiting vendors from placing on the market certain batteries and accumulators with a proportional mercury or cadmium content above a fixed threshold. Directive 2006/66/EC, which replaces an older EU batteries directive, also promotes a high rate of collection and recycling of waste batteries and accumulators. It aims to improve the environmental performance by all parties involved in the life cycle of batteries and accumulators, including their recycling and disposal.

The EU member states transposed the directive as of Sept 28, 2008, and it applies to all types of batteries and accumulators, except for those used in equipment to protect EU countries' security or for military purposes or in equipment for use in space.

As with the WEEE (waste-electrical-and-electronic-equipment) directive, producers must label batteries and accumulators with the crossed-out wheeled-trash-bin symbol, meaning that users cannot dispose of these items in the trash, and the labels must list the chemicals present in batteries and accumulators.

The New Batteries Directive should affect electronics manufacturers because they will have to design and manufacture electronics end products in such a way that users can easily remove the battery.

For more on the new battery directive, see www.edn.com/blog/570000257/post/270032227.html.

OUTLOOK

SENSORS TO DRIVE GLOBAL MEMS MARKET TO $8.8 BILLION IN 2012

The global market for MEMS (microelectromechanical systems) will expand to $8.8 billion in 2012, up from $6.1 billion in 2006, according to data from iSuppli Corp (www.isuppli.com).

"The markets for mainstay MEMS-actuator products—ink-jet heads and DLP [Digital Light Processor] chips from Texas Instruments Inc—finally have passed the baton to MEMS sensors to drive the next growth wave in the market," says Jérémie Bouchaud, iSuppli's director and principal analyst for MEMS.

ISuppli reports that part of the growth is the result of the rapid rise of consumer-electronics applications, such as motion sensors for gaming, laptops, and digital still cameras.

"Mobile handsets will also be a strong area, with MEMS-sensor revenue in this area to rise at a 22.9% CAGR to reach $925 million in 2012," Bouchaud says.

Together with consumer electronics, the mobile handsets, automotive, and industrial-process-control segments will account for more than 60% of total MEMS-market revenue in 2012, the market-research company forecasts.

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The Impact of

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THE GREENING OF THE SUPPLY CHAIN

A Letter from the Editor

It started two years ago with the European Union's Restriction on Hazardous Substances (RoHS) and it's literally sweeping the globe. "It" is the environmental movement, and no one in the electronics industry doubts it is here to stay.

The electronics industry in particular is the subject of many of these environmental mandates—one of the "Es" in "WEEE" stands for "electronics" and the so-called "China RoHS" targets "electronic information" products. Why the bad rap? The short lifecycle of many consumer electronics products means cell phones, PCs and Internet appliances are hitting landfills at an increasing rate. The rapid development of China—now one of the biggest manufacturing centers in the world—has added to air pollution problems in that region. So governments are no longer making recycling and eco-friendly designs voluntary: they are a requirement for doing business in a global economy.

Electronics distributors are only one part of the supply chain that makes electronics manufacturing possible (and cost-effective). Although distributors are not directly responsible for ensuring products comply with local environmental mandates, they are the conduit of compliance information from the supplier to the end customer. The sheer volume of products passing through the channel makes it imperative that distributors are up-to-date on every law affecting their customers' business.

Distributors have stepped up to the task, gathering compliance information from suppliers or directing customers to relevant supplier information. In cases where compliant and noncompliant products might get mixed up, the channel has developed inventory-management systems that prevent such mistakes. And many companies have taken green one step further, by embedding sound environmental practices into their corporate cultures. The "greening" of the electronics supply chain is well underway.

There are still a lot of questions surrounding the environmental movement; among them, what products will be affected by China's evolving mandate? Once that information becomes available, customers of the global supply chain can be assured their distributors will have it handy. "If distributors don't have the information themselves, they know where to direct the customer to find it," says Barney Martin, vice president for industry practices for the National Electronic Distributors Association. "When you get right down it, [managing such information] is all about customer service."

This supplement—both in print and an expanded online version—is designed to be a resource for all companies playing in the global supply chain. Much of the information has been contributed by distributors. We encourage readers to take a look—and "happy greening!" ■

Freelance writer Barbara Jorgensen has been covering the electronics distribution industry for nearly 20 years, most recently as a Senior Editor at Electronic Business magazine.

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EDN Worldwide
Russ Pratt, EDN Group Publisher
Phone: 781-734-8417 Fax: 781-734-8070
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Judy Hayes, Associate Publisher
judy.hayes@reedbusiness.com

Regina Twiss, CPS Manager
reginatwiss@comcast.net

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The Impact of
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GREEN
TAKES ROOT IN ELECTRONICS INDUSTRY

Distributors adapt to a rapidly changing compliance environment

July 1, 2006 was a milestone in the annals of the electronics industry. That day, lead, mercury, cadmium and certain flame retardants were officially banned from electronics products entering the European Union. But even as the EU's Restriction on Hazardous Substances (RoHS) became law, detractors of the mandate figured RoHS was a paper tiger: heavy on political correctness but light on actual implementation.

Two years later, there's little question that the EU takes its environmental laws seriously. Several measures have joined RoHS in the EU's movement toward "green." Other countries—specifically, China and Korea—are releasing their own environmental standards. EU enforcement bodies have prosecuted at least four RoHS-noncompliance complaints and investigated many others. "As far as the world going 'green' it's not a matter of 'if,'" says Ken Stanvick, principal of consultancy Design Chain Associates, "it's a matter of 'when.'"

Georg Steinberger, vice president of communications for Avnet Electronics Marketing EMEA and director of Avnet's green efforts.

Environmental statutes will continue to add complexity to the global electronics supply chain. The sheer volume of information alone required of component suppliers and their distributors is staggering. "RoHS compliance doesn't mean you check off a 'yes' or 'no' box on a form to declare your products are compliant," says Georg Steinberger, vice president of communications for Avnet Electronics Marketing EMEA and director of Avnet's green efforts. "You have to know what materials are contained within the products you ship and be able to document those contents."

The channel has invested in personnel, IT and facilities to identify, track, store and ship both RoHS-compliant and noncompliant components. (Noncompliant components are still in demand because some electronics are exempt from RoHS.) Overall, the global electronics industry spent $32 billion initially to comply with RoHS, according to a survey conducted by researcher Technology Forecasters Inc. Distributors have also stepped up their engineering assistance to aid designers with component selection, materials compatibility and product lifecycle issues. But have these measures prepared the channel for the next wave of green legislation?

"There are no standards per se that define exactly what 'green' is," says Stanvick. "There's no consistent methodology around the globe." Still, the supply chain is responding to both the challenges and opportunities of an increasingly green world.

RoHS: Just the Beginning

When the calendar flipped to July 2, 2006, the electronics supply chain did not grind to a halt. In fact, two years down the road, the distribution industry is beginning to breathe a sigh of relief. "The biggest problem for distribution was mixed stock," says Gary Nevison, director of legislation and environmental affairs for Newark and Farnell, "and that is smoothing out a bit." But July 2006 was just the beginning. The EU is currently reviewing the RoHS mandate with an eye toward expanding its reach. Experts say it's very likely that certain classes of electronics products originally exempt from RoHS—medical equipment and monitoring and control instrumentation—will have to comply in the future. "Medical and test equipment were exempt because the reliability of unleaded solder was uncertain," says Nevison. "Today, more people are comfortable with [unleaded]."

Gary Nevison, director of legislation and environmental affairs for Newark and Farnell.

Nevison and others say the expansion won't negate the channel's RoHS efforts. However, a revised RoHS may also seek to ban more substances than those currently cited in the mandate. This may become a huge undertaking because RoHS requires the materials content of an electronics product be declared and documented. "Getting materials information out of suppliers was a nightmare for distributors two years ago," says

Nevison, "and it will a nightmare when a revised RoHS takes effect."

"You have to keep in mind that the migration from RoHS compliant products to noncompliant occurred over a varying time scale," says Brian McNally, president for Arrow Electronics Global Alliance and Supply Chain business. "There were pockets of demand all over the world [for both types of components] and managing that was a challenge."

RoHS Part Deux

Distributors and design engineers will face many of the same challenges with an expanded EU RoHS: components containing the banned materials will eventually become obsolete. Lead-free solders may still pose some performance risk—these solders melt at very high temperatures and heat can damage many types of components. Distributors will have to obtain and stock newly compliant components. "Two years ago, distributors had a lot of both compliant and noncompliant stock in the warehouse," Nevison points out, "and that's a huge financial burden."

A cascading wave of environmental mandates in other regions of the world creates another problem: RoHS compliance doesn't mean your product will be compliant worldwide. Although China's and Korea's environmental mandates closely resemble RoHS, each contains significant differences. China's two-phase Administrative Measure on the Control of Pollution Caused by Electronic Information Products (referred to as "China RoHS") covers a wider product scope; requires specific labeling; and calls for mandatory inspection and testing. Currently in its first phase, China RoHS does not yet restrict substances but requires the presence and amount of hazardous materials be declared on a label. If such substances are present, that label must show where the hazardous materials are located in the product.

The second phase of China RoHS is expected to restrict substances in certain products. These products, along with enforcement dates, will be specified in a catalog scheduled to be published in late 2008. At this stage, testing and certification will be compulsory.

The testing and certification requirement could create a bottleneck in the electronics supply chain, experts say. Products exported to China must be tested and accredited by Chinese test houses. A smooth transition will depend on the efficiency of the authorized test houses and the number of products that appear in the first catalog.

Korea's Act for Resource Recycling of Electrical/Electronic Products and Automobiles ("Korea RoHS") has already been adopted in South Korea. The act restricts hazardous materials; requires products be designed for efficient recycling; and mandates the collection and recycling of electronic waste. The scope for electrical products includes TVs, white goods, air conditioners, PCs and peripherals, and mobile phones. The directive also covers automobiles.

Korea RoHS emphasizes the strict limitation of hazardous substances and design for easy recyclability.

Another mandate on the industry's radar is the EU's Registration Evaluation Authorization (and restriction of) Chemicals. REACH, which was implemented in June 2007, requires manufacturers and importers of chemicals and preparations (ink, paint, varnish, cleaning agents, fluxes, etc.) register these substances and provide directions for their safe use. Many of the 30,000 substances targeted are used in electronics products.

This is an enormous undertaking, says Nevison. "Today there is no safety data outlining the risks on 21 percent of the chemicals used in high volume across the EU, and inadequate data on a further 65 percent," he says. "REACH takes a completely different approach to substances than RoHS."

In other words, eco-compliance is a moving target. Distributors have been addressing the rapidly changing environment by ensuring their IT systems are flexible. "Even before RoHS was official we were starting to think about IT tools that don't just manage the compliance data we know, but can integrate future changes," says Avnet's Steinberger. "You start with RoHS, WEEE, the battery directive and REACH and make sure you have a data management system that links a part number to all the other information the customer needs."

Even those part numbers, however, pose a challenge. Not every supplier has created a new part number to identify RoHS-compliant parts. Distributor computer systems have difficulty differentiating compliant and noncompliant devices, which needed to be stored separately. Newark and other distributors have established internal numbering schemes to sort both kinds of products. "It was an absolute nightmare," says Nevison. "It was also the best decision we ever made."

Opportunities and Challenges

Distributors' ability to manage such mountains of data has served the channel well. "We have been able to build some excellent core processes to ensure we have good data and we will be able to build on that," says Arrow's McNally.

"If we can provide information to customers in a professional and straightforward manner it

helps secure your position in the marketplace," says Steinberger.

However, distributors are looking for more ways to service customers in the rapidly changing environment. One way is by assisting engineers in designing eco-friendly products. The EU's Waste Electrical & Electronic Equipment (WEEE) Directive—which was implemented this year—is closely associated with RoHS. WEEE requires 10 categories of electrical and electronic equipment to be collected, treated, recycled and disposed of when it reaches end-of-life. "Engineers now have to think about product design in terms of making the entire product recyclable," Nevison says. Along those lines, Newark recommends measures such as substituting plastic clips for screws; labeling larger plastic parts, such as enclosures, with the type of plastic (and flame retardant) used; and avoiding metal inserts in plastic moldings.

The Energy-using-Products Directive (EuP), which became EU law in November 2005, is a huge opportunity for distributors. EuP aims to improve the energy efficiency of electric/electronics devices throughout the product life cycle. EuP's focus is on the design phase since design determines what resources will be used during a product's lifetime. Some components, for example, are more energy efficient than others. Because distributors are privy to their suppliers' product development roadmaps, the channel is in a good position to help engineers choose energy-efficient components and designs.

"Where you had a technical sales force driven by a supplier to provide a product, you now have FAEs driven by lifecycle management and eco-friendly design. EuP is an integrated policy that follows a product from the design to the dumpster," says Steinberger. "You have to make sure all the issues are covered from the materials used to recycling and energy efficiency. This is where our engineering know-how comes into play with customers."

Newark, for example, recommends engineers design equipment with good ventilation and low power dissipation to avoid the need for power-consuming fans. The power consumption of ICs and other components varies considerably and that information can be hidden in lengthy data sheets. Distributors can help engineers select low power consumption components. Other tips from Newark include:

- *Using lower voltages. Power consumption is directly proportional to voltage and so halving voltage halves power consumption.*
- *Using LCD rather than CRT displays. LCDs also use less power than LED indicators or filament lamps.*
- *Using switch-mode power supplies instead of linear power supplies (lower power and work off a wider voltage range).*

Many in the channel believe these services are only the tip of the iceberg. DCA's Stanvick says many small companies don't have the means to develop their own compliance-assurance systems and are looking to outsource that function. "We have been approached for help on WEEE, special packaging and labeling things and lifecycle management," says Avnet's Steinberger. "We are always anticipating what the customer will expect so we'll be able to offer it as an add-on."

Distributors, of course, would like to charge for such add-on services. But experts say that might be difficult. "One point of view is, you are taking something you have to do and spinning it as something you are willing to do," Stanvick says. "These environmental laws aren't voluntary—this is the way things are going to be." ■

More EU Eco-laws

In addition to RoHS, WEEE and REACH, the European Union has two other environmental mandates to keep an eye on:

ATEX Directive: The ATEX Directive (from the French ATmospheres EXplosible) is in fact two complementary directives. ATEX 137 is the Worker Protection Directive and ATEX 95 the Equipment Directive.
The ATEX scope includes any equipment that is used where there is a risk that the atmosphere will contain flammable or explosive mixtures of air and gases, mists, dusts, vapors etc. New and used equipment and some types of components, such as relays, need to comply. ATEX took effect in 2003.

Batteries Directive: The Batteries Directive aims to make businesses that produce and sell batteries responsible for collecting and recycling at end-of-life. EU member states are expected to adopt the measure by Sept. 28, 2008. Batteries containing more than a trace of cadmium will be banned except in emergency alarm systems, medical equipment and cordless power tools. It is likely that some types of nickel cadmium batteries will become obsolete. Also, batteries must be clearly labeled to show how long they will last from 2009, allowing consumers the opportunity to compare cost versus lifespan.

Additionally, Australia and Norway are considering their own environmental mandates and individual states in the U.S. have passed legislation.

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Avnet Green Initiative

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*As rated by Hearst Electronics Group: The Supplier Interface Study, 2007.

WHERE TO GO FOR GREEN

The following is a sampling of Websites and organizations that provide information or services associated with international environmental mandates. This is not meant to be a comprehensive list.

GENERAL INFORMATION

The Blue Book
http://ec.europa.eu/enterprise/newapproach/legislation/guide/document/1999_1282_en.pdf

The EC's guide to the implementation of directives based on a global approach to environmental safety.

Department of Toxic Substances Control
http://www.dtsc.ca.gov/HazardousWaste/RoHS.cfm

The DTSC aims to protect Californians from hazardous waste.

Eco-Frontier
http://www.kece.eu/data/Korea_RoHS_ELV_April_2007_EcoFrontier.pdf

Translates and analyzes Korea's environmental initiatives.

The European Commission for the Environment
http://ec.europa.eu/environment

The European Commission's Environment Directorate-General (DG) initiates and defines new environmental legislation. It provides detailed information about all EU environmental mandates including RoHS, WEEE and REACH.

Greensupplyline.com
http://www.greensupplyline.com

Compiles news and articles about a variety of environmental initiatives.

REACH News
http://www.reach-news.net

Information and news on the EU's REACH mandate.

RoHS Home Page
http://www.rohs.gov.uk

Information on RoHS, exemptions, amendments, news.

RoHS and WEEE News
www.rohs-news.com

News articles from a variety of sources about ongoing environmental developments.

CONSULTANCIES

Agile Business Consultants
http://www.pb-free.info

Provides information and services on RoHS and WEEE compliance.

Design Chain Associates
www.designchainassociates.com

DCA is a consultancy to the electronics industry and provides services on supply chain management; environmental issues, anti-counterfeiting and other industry issues.

Elfnet
http://www.europeanleadfree.net/default.asp

ELFNET (European Lead Free soldering NETwork) is a European research network of the national organizations, technical experts and industry bodies in micro-electronics. ELFNET enables electronics producers in the EU to meet an EU directive to introduce lead-free soldering.

EMSL
www.emsl.com

An environmental testing firm providing analytical testing services to support environmental investigations focused on asbestos, microbiology, lead paint, environmental chemistry, indoor air quality, industrial hygiene and food testing.

Envirowise
http://www.envirowise.gov.uk/page.aspx?o=electronics

Envirowise is a government funded organization that offers UK businesses free, independent, confidential advice and support on ways to reduce environmental impact.

EPPA
http://www.eppa.com

Assists clients with management of the risks and opportunities resulting from the European political, regulatory and socio-economic landscape.

Grace Compliance Specialist
http://www.graspllc.com/China%20RoHS%20Standards%20-%20Limits.php

Provides news and information about China RoHS.

IMR
www.imrtest.com

Offers materials research and testing services, including failure analysis, expert testimony, lab management, product testing, training.

Intertek
http://www.intertek-rohs.com

Provides compliance assistance with RoHS, WEEE, REACH, California Proposition 65, China RoHS, Korea RoHS, EuP, Japan Green (JGPSSI) , and other mandates.

Lead Out Project
http://www.leadoutproject.com/main_h/index.asp?p=9>LEADOUT

A European funded project on lead-free technologies. The main objective of the project is to provide technical support to a wide range of electronics manufacturers in Europe.

Q Point Technology
www.qpointtech.com

Provides engineering and information assistance to meet environmental compliance regulations.

REACH Impact
www.reachimpact.com

Provides a methodology for REACH compliance.

Soldertec
www.lead-free.org

Soldertec is a business providing laboratory testing, troubleshooting, and analytical services to the global electronics industry.

Technology Forecasters Inc.
www.techforecasters.com

TFI is an industry consultancy specializing in electronics manufacturing services and provides guidance and implementation support for corporate-wide environmental best practices.

INDUSTRY ORGANIZATIONS

AeA
http://www.aeanet.org

Information on environmental legislation affecting the electronics industry. Includes a translation of China RoHS.

Electronics Industries Alliance (EIA)
www.eia.org

Information on environmental legislation affecting the electronics industry.

International Electronics Manufacturing Initiative (iNEMI)
www.inemi.org

An industry-led consortium of approximately 70 electronics manufacturers, suppliers and related organizations.

IPC
www.ipc.org

IPC is a global trade association dedicated to furthering the competitive excellence and financial success of participants in the electronics industry.

National Electronics Distributors Association (NEDA)
www.nedassoc.org

NEDA is a not-for-profit trade association representing companies involved in the supplier authorized distribution of electronic components and parts, computer and computer peripheral components and test, measurement and control equipment; and their suppliers.

Semiconductor Industry Association (SIA)
www.sia.org

The premier trade association representing the U.S. semiconductor industry.

INTERNATIONAL TRADE ASSOCIATIONS

European Electronic Component Manufacturers Association - European Semiconductor Industry Association (EECA-ESIA)
http://www.eeca.org

To promote and defend the vital interests of the European electronic components industry.

Japan Electronics and Information Technology Industries Association (JEITA)
http://www.jeita.or.jp

The objective of the Japan Electronics and Information Technology Industries Association (JEITA) is to promote the healthy manufacturing, international trade and consumption of electronics products and components.

Korean Semiconductor Industry Association (KSIA)
http://www.ksia.or.kr

Formed to promote the cooperation and the development of Korea's local semiconductor industry.

Taiwan Semiconductor Industry Association (TSIA)
http://www.tsia.org.tw

Formed to promote the cooperation and the development of Taiwan's semiconductor industry.

COMPLIANCE/ENFORCEMENT

Environmental Compliance Assistance Centers
http://www.assistancecenters.net/about/index.cfm

The Environmental Protection Agency (EPA) has sponsored partnerships with industry, academic institutions, environmental groups, and other agencies to launch the centers. The centers help businesses, local governments, and federal facilities understand federal environmental requirements and save money through pollution prevention techniques.

ERA Technology
http://www.era.co.uk

A list of the RoHS enforcement bodies by country.

National Printed Wiring Board Resource Center
http://www.pwbrc.org

Established by the National Center for Manufacturing Sciences (NCMS) in partnership with the IPC, and funded from the U.S. Environmental Protection Agency (EPA). The PWBRC provides easy-to-use, in-depth technical information on pollution prevention and regulatory compliance.

National Weights and Measures Laboratory (UK)
http://www.nwml.gov.uk/Content.aspx?SC_ID=3

Enforces RoHS compliance in the U.K.

RoHS Group
http://www.rohs.gov.uk/content.aspx?id=14

A cooperative initiative of organizations providing RoHS conformity programs and support.

SGS Group
http://www.rohs.sgs.com

Provides testing and certification services of electrical, electronic and telecommunication equipment.

TUV Rheinland
http://www.us.tuv.com

Provides technical services worldwide to achieve sustained development of safety and quality.

INSIDE GREEN AND OUT

Distributors embrace eco-culture

For many distributors, "green" reaches far beyond shipping eco-friendly components to their customers.

"Newark believes green extends beyond our responsibility to the electronics industry—we see it as part of our social responsibility," says Barry Litwin, senior vice president for marketing at Newark. "Aside from improving our competitiveness, we see it as a sound business practice."

To varying degrees, distributors have embedded green into their corporate culture, practicing everything from paper and package recycling to reducing their company's carbon footprint. "In order to have any credibility in [the environmental] area, we have to walk the walk and talk the talk," says Georg Steinberger, vice president of communications for Avnet Electronics Marketing EMEA and director of Avnet's green efforts.

A company's environmental policies also make a difference in the workforce, distributors say. "People are making this part of the criteria of who they are going to work for," says Steinberger. "It's not just the money and the job and the traditional aspects—it's also how a company behaves that is becoming important."

At the same time, distributors are cognizant of the impact the environmental movement has on their business. Increasingly, businesses want to partner with companies that are seen as green. "We get [environmental] questionnaires from suppliers and we are seeing more of our customers making [green] a requirement of doing business," says Ken Manchen, Newark's director of environmental affairs. "You also see Top 100 companies such as HP that have embraced this goal and they quiz us more than anyone."

The investment community is also rewarding companies with a good eco-track record. Newark is a member of the FTSE4Good Index of Corporate and Social Responsibility and has participated in the Business in the Environment regional survey of Corporate Environmental Engagement every year since its inception and has shown continual progress, increasing its score by 5 percent in the latest survey.

Barry Litwin, senior vice president for marketing at Newark.

Has the channel been able to capitalize on green? Executives say it is difficult for a number of reasons to tie environmental compliance efforts directly to the bottom line. At the onset of RoHS, says Brian McNally, president, Arrow Electronics Global Alliance and Supply Chain, savvy inventory management created opportunities. "If you could see how demand for RoHS compliant and noncompliant parts was shifting, you could position your noncompliant products based on the expected demand and therefore create a market for yourself."

Another opportunity, McNally says, is the data management resources distributors built. Arrow took a pro-active approach in gathering as much data as possible from its more than 600 suppliers and vendors it's not franchised with. Customers that use Arrow's online tool for bill of material (BOM) scrubbing need information for the entire BOM, not just the portion it buys from Arrow,

How Newark is Going Green

Among the efforts Newark is taking toward its internal environmental goals:

Measuring, since 2002, items such as carbon emissions and recycled content.
Setting up green teams within its facilities that chart things such as emissions and energy costs.
Being audited by a third-party energy expert.
Reducing the amount of paper it uses in printing its catalog. "We are setting minimum standards of 2,500 pages a year and will augment that with Web-based catalogs and e-mail to our customers," says Barry Litwin, Newark senior vice president of marketing. Newark is also reusing packaging from suppliers and no longer uses packing peanuts.

Newark's overall goals include:
- Reducing CO2 emissions by 3% by 2008 (versus 2006 base year)
- Reducing CO2 emissions by 10% by 2010 (versus 2006 base year)

Results include:
- 2,700 metric tons of waste is annually being recycled
- This figure represents 63% of company waste

Source: Newark Electronics

The Global Environmental Regulation coverage continues online…

visit: www.edn.com/greeninthechannel

Risky Business:
Channel Helps Ensure Compliance
At the time the European Union's Restriction on Hazardous Substances (RoHS) became law, there were still a lot of outstanding questions about who exactly is going to enforce this law. *EDN* takes a look at the level of enforcement taking place across the globe.

What Does Green Mean?
Standards Would Assist the Channel's Compliance Efforts
Wading through the alphabet soup associated with environmental compliance is daunting for many companies. Industry experts say two words: "Standards" and "simplify" would help, but no one standards body oversees global mandates.

says McNally. "At the time of the transition to RoHS, many customers and suppliers were looking for good BOM information and we were able to sell more seats for our online subscription services."

Sager Electronics is targeting opportunities in the growing clean-energy market: companies developing alternative energy solutions and emission-reduction technologies. "Sager wishes to invest time on behalf of ourselves and our suppliers in those manufacturers who are inventing things that solve the world's problems, and provide those engineering solutions to long term big picture problems," says Faris Aruri, vice president for corporate marketing. "With rising fuel costs and climate change, many are calling for wind, sun, and other earth friendly energy sources. Some have estimated the cost of transforming the nation to clean energy at $3 trillion over the next 30 years. Huge investments will have to be made in technology."

Still, industry experts say it'll be tough to build a competitive advantage around eco-friendliness. "None of the environmental mandates adopted so far are optional. So for any company in the supply chain, it's hard to claim there's an advantage to being 'more' compliant," says Arrow's McNally. "We see offering compliance services as part of our job."

"We have been able to build some excellent core processes to ensure we have good data," he adds. "We can leverage what we have learned from our prior experience and build on that. This isn't going to go away; [environmental mandates] are only going to add more complexity to the supply chain." ■

productroundup

DISCRETE SEMICONDUCTORS

Power MOSFETS provide fast switching for high-side-MOSFET applications

The vendor's line of synchronous dc/dc converters now includes the TPC80xx power MOSFETs suiting high-side-MOSFET applications and enabling a lower gate charge and a lower gate resistance. The TPCM8004 features 30V maximum drain-to-source voltage, 24A maximum drain current, 11-mΩ maximum on-resistance, 1Ω typical gate resistance, and a 3.5×4.65×0.75-mm TSSOP package. The TPC8030-H and the TPCA8031-H have 30V maximum drain-to-source voltage, 24A maximum drain current, 11-mΩ maximum on-resistance, and 5×6×0.95-mm SOP packages. The TPC8037-H and the TPCA8038-H high-side MOSFETs have 30V maximum drain-to-source voltage, 12A maximum drain current, 11.4-mΩ maximum on-resistance, and 5×6×1.6-mm SOP-8 packages. The TPC8030-H and the TPC8037-H have 1Ω gate resistance, and the TPCA8031-H and the TPCA8038-H feature 3.4Ω gate resistance. The TPC80xx dc/dc converters cost 52 cents.
Toshiba America Electronic Components, www.toshiba.com/taec

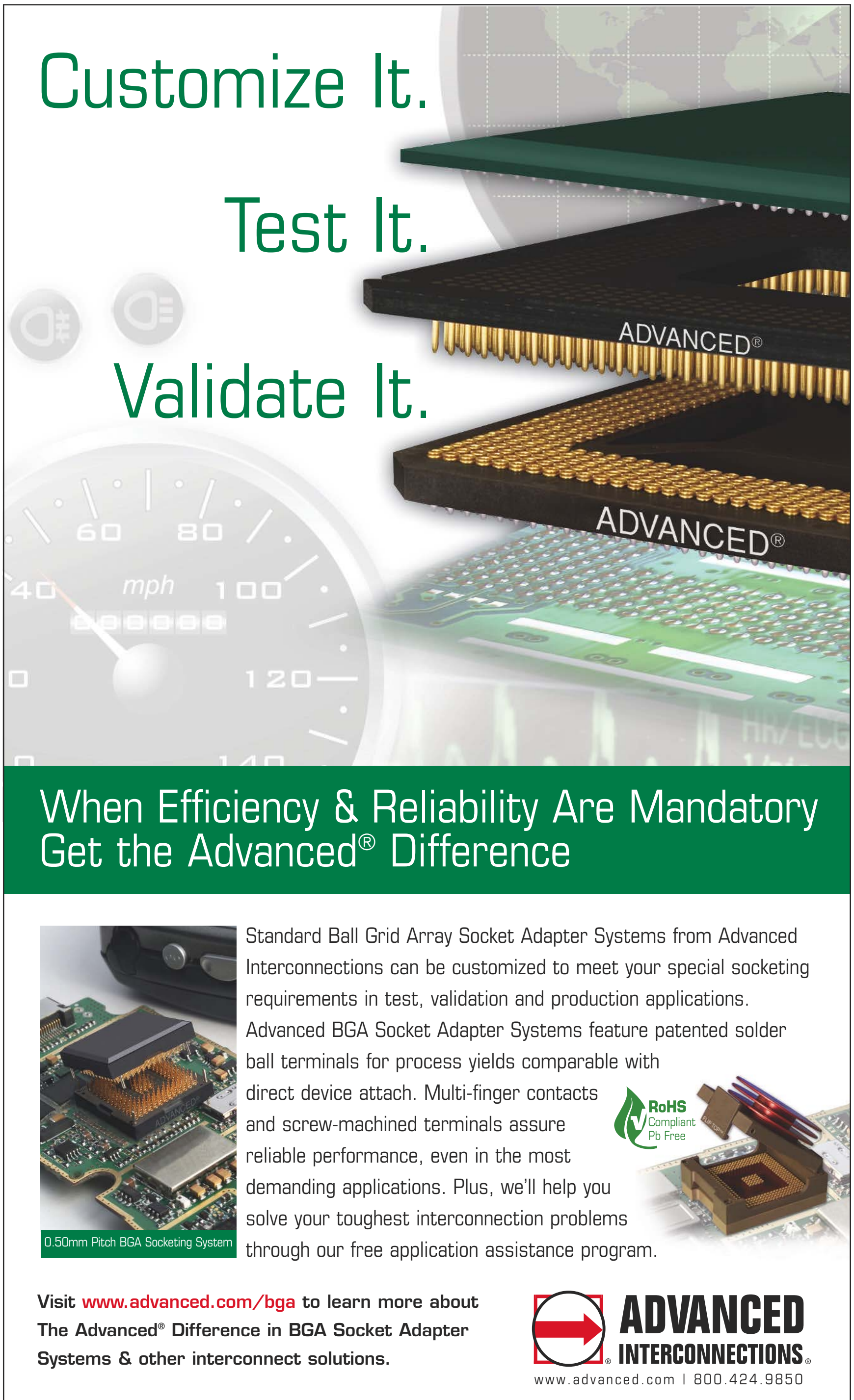
Rugged, 600V ICs are automotive-qualified

The rugged AUIRS212xS family of single-channel high-side-driver ICs aims at low-, midrange-, and high-voltage-automotive applications, such as automotive drives, high-voltage actuators, and fuel-efficient direct-injection systems. The AUIRS2123S and the AUIRS2124S high-speed power MOSFETs and IGBT drivers have a 10 to 20V gate-drive supply range. The output drivers include high-pulse current-buffer stages for minimum driver cross-conduction, and the floating-channel drives N-channel power MOSFETs or IGBTs in the high-side configuration, operating as high as 600V. The AUIRS2123S has output signals in phase with the input signal, and the AUIRS2124S provides output signals out of phase with the input signal. Both devices provide UVLO protection and CMOS-Schmitt-triggered inputs with pull-down. Available in a lead SOIC-8 package, the AUIRS212xS costs 72 cents (100,000).
International Rectifier, www.irf.com

8, 12, and 16A triacs come in isolated TO220 packages

The BTAxxxx series includes 12 triacs with 8, 12, and 16A available power ratings and gate-trigger currents of 35 and 50 mA. The series suits industrial and control applications with critical isolation-voltage and safety requirements. Features include an 800V blocking voltage, a 16A-rms on-state current rating, and 2000V/μsec immunity to dV/dt. Available in isolated TO220 packages, the BTAxxxx triacs cost 45 cents for the 8A version, 47 cents for the 12A version, and 54 cents for the 16A version (1000).

On Semiconductor, www.onsemi.com



MOSFET integrates ribbon bonding with surface-mount power package

The 250A STV250N55F3 power MOSFET combines ribbon bonding with a surface-mount power package to deliver 1.5-mΩ on-resistance with the ability to handle high currents for 55V applications. The MOSFET operates at temperatures as high as 175°C, making it suitable for use in high-current electric-traction applications, including fork-lift trucks, golf carts, pallet trucks, lawnmowers, and wheelchairs. The device dissipates 300W at 25°C and has a 200A continuous-drain current. The STV250N55F3 costs $2.50 (10,000).

STMicroelectronics, www.st.com

MOSFET line has low on-resistance

The Siliconix 8 to 30V P-channel PowerPack SC-75 power MOSFETs provide 0.052Ω on-resistance, and the 8V devices provide gate-to-source-voltage on-resistance as low as 1.2V. The line also includes the single SiB411DK and dual SiB911DK 20V devices. The single device has an on-resistance of 0.052 to 0.066Ω at a 4.5V gate drive. The SC-75 devices come in 1.6×1.6-mm-footprint packages, and prices range from 10 to 15 cents (100,000).

Vishay Intertechnology, www.vishay.com

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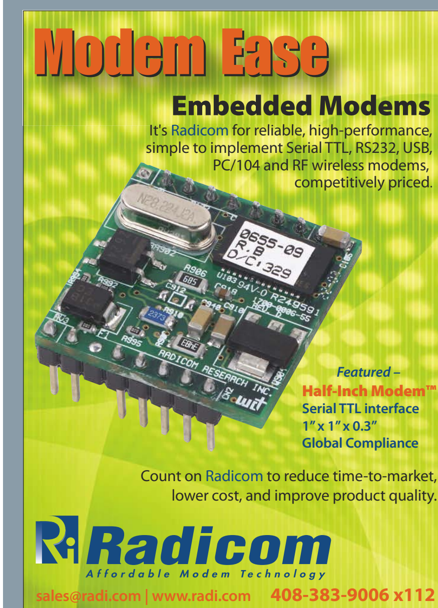

Repeat offender

DANIEL VASCONCELLOS

A few years ago, I designed a multiplexer that interfaced four T1 twisted-pair telephony lines to optical fiber. The integrated-CMOS T1 line drivers automatically generated the correct analog pulse waveshape to satisfy the Bellcore pulse mask requirements. Their only problem was they were somewhat picky about the termination impedance: More than 10% termination mismatch away from 100Ω and they complained by producing a distorted pulse shape that no longer agreed with the mask. The greater the impedance mismatch, the more distorted the pulse shape. This behavior was not a big deal; it is usually easy to match line and termination impedances to better than 10%.

All our prototypes were working fine until the day we obtained some T1 repeaters from a well-known manufacturer and attempted to drive their receivers with our prototypes. Our transmitted pulse waveform was almost unrecognizable on the scope; it looked just like it was driving into an open circuit.

I called the repeater manufacturer, and a support engineer assured me that the repeaters had an input impedance of 100Ω. He added that, when their other customers complained about similar problems, the standard approach was to tell them to add a 100Ω resistor across the receiver input.

I pointed out that this approach would result in a 50Ω termination and make things worse. If other customers were having similar problems, then maybe something was wrong with the repeater design. The engineer insisted that there was nothing wrong with it; all their lab tests had shown that the "active termination circuitry" worked properly. But he did say he would look into it some more.

In the meantime, my boss was somewhat upset that I could not make our product work with these repeaters. I demonstrated that our product worked nicely with 100Ω termination, and because it did not work with the repeaters there must be a repeater problem. The boss could not accept this hypothesis.

About a week later, the repeater manufacturer engineer called me back and explained that improperly loaded CMOS drivers could be responsible for the pulse distortion. He also explained that this problem had not shown up with older driver designs that used RC waveshaping networks. He then sheepishly admitted that the company's production department had made a vendor change for a FET in the active input-termination circuit. The new FET package had a different lead arrangement that production didn't notice at the time of substitution. Hence, all the repeaters the company had shipped since the vendor change did *not* present a 100Ω termination to the line, and production testing did not include input-impedance measurement. Oops!

I offered to fix our repeaters myself if he could send the new FET-pinout arrangement, but he insisted that we return the repeaters to the company for rework. We did, and our product then worked great.

The only problem we had after that situation was that a Baby Bell telephone company evaluated a product sample and complained about the transmitted pulse shape. Whoever had wired the central office made the mistake of using 72Ω twisted pair instead of the standard 100Ω cable. EDN

You can reach design consultant Glen Chenier at glen@teetertottertreestuff.com. Like Glen, you can share your Tales from the Cube and receive $200. Contact edn.editor@reedbusiness.com.

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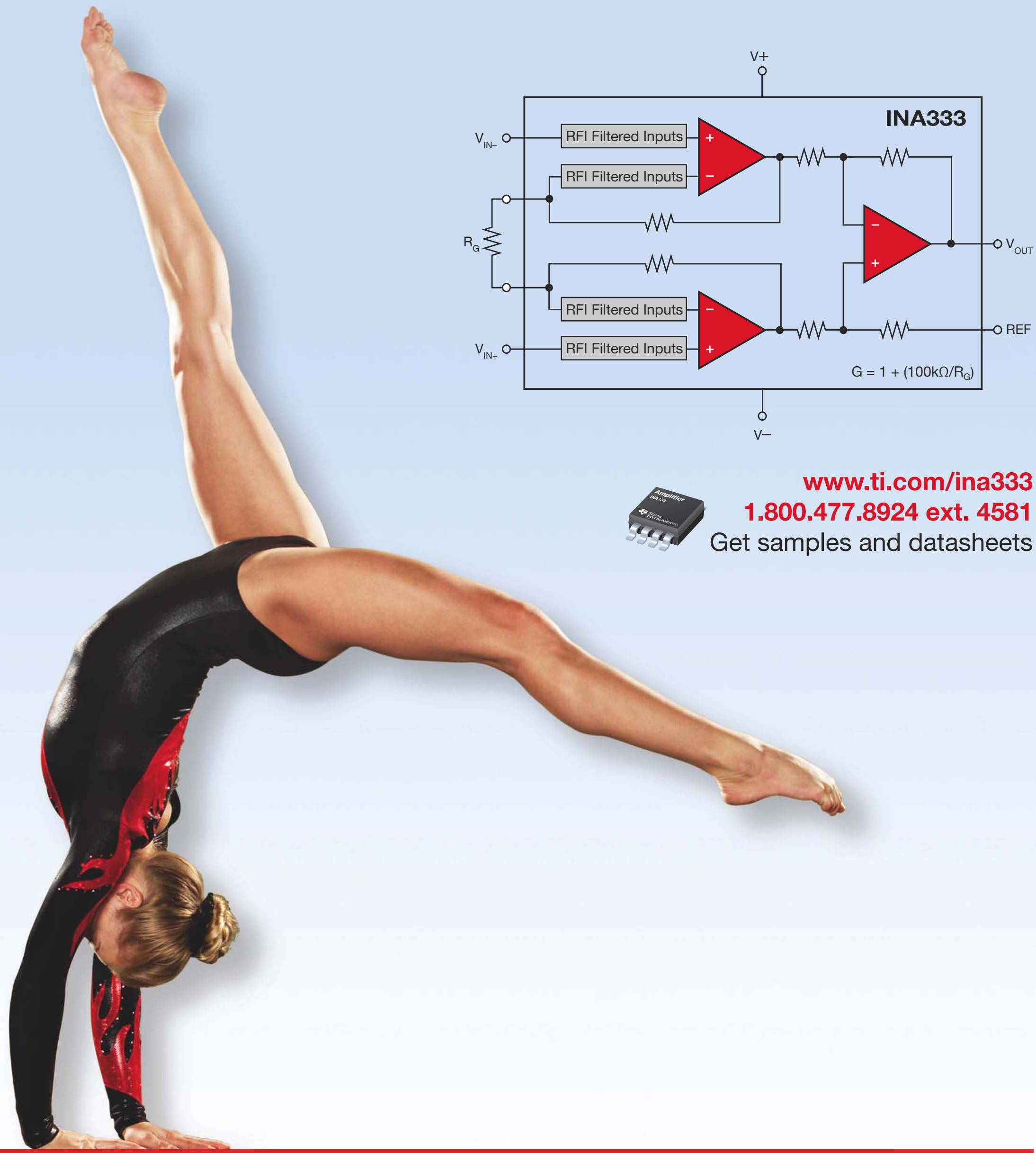

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